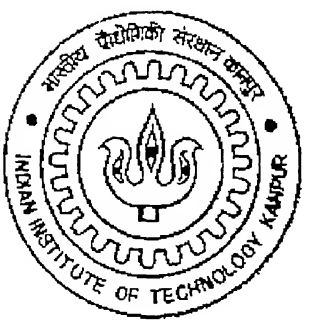
Characterization of silicon oxynitride grown by oxidation of silicon in nitrous oxide.

A Thesis Submitted in
Partial Fulfillment of the Requirements for the Degree of
Master of Technology

By

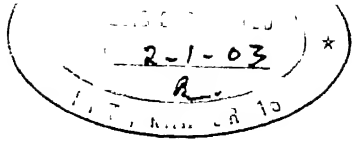
Amitesh Shrivastava



To the

DEPARTMENT OF MATERIALS AND METALLURICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
January, 2003

CERTIFICATE



This is to certify that the work contained in the thesis entitled **"Characterization of silicon oxynitride grown by oxidation of silicon in nitrous oxide."**, by Amitesh Shrivastava, has been carried out under my supervision and this work has not been submitted elsewhere for a degree.

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Acknowledgements

I take great pleasure in writing this acknowledgement page to thank all those individuals who helped me to complete this thesis successfully and for making my stay here, at IIT Kanpur, a memorable one.

With due respect, I express my sincere gratitude to Dr. Deepak Gupta and Dr. Monica Katiyar for their invaluable guidance and encouragement during the course of this thesis work. Discussions with them have aided a lot in structuring and cohering the thoughts to give a good shape to this work.

I am also thankful to Dr. Narain and Dr. Satyendra Kumar for providing moral and technical support during the course of the thesis.

I express my deep indebtedness to my friend's Surendra and Sanjay for their moral support and encouragement during my stay at IIT. Discussions with them, although sometimes led to serious altercations, have helped me to get out of my troublesome moments and bitter experiences in IIT.

I express my deep sense of gratitude to Rohit and Siddharth for helping me to acquaint with the experimental equipment and giving final shape to this thesis. Thanks are also due to Tripathiji, Vajpayeeji and other staff members for their help during the experimental work.

I am thankful to my dear lab mates Amit, Aditya, Asha, Himanshu, Nitesh, Pawan and Saswat for maintaining a cordial and friendly environment throughout the course work and thereafter. I would also like to extend my sincere thanks to all those who directly or indirectly helped me throughout my stay at IIT Kanpur.

Amitesh Shrivastava

Abstract

SiO_2 has traditionally been the oxide of choice for MOSFET devices, but for sub 0.25-μm ULSI technology the search for alternative oxide started more than a decade ago. The motivation is to find a material superior than thin SiO_2 in terms of (i) impurity penetration through the oxide, (ii) reliability, (iii) leakage current, and (iv) uniform deposition. It has been shown that silicon oxynitride (SiO_xN_y) does not only improve the reliability but also suppresses the boron penetration from the gate electrode The focus for this study is to extend the applicability of this material to even smaller devices by depositing it at lower temperatures, and making sure it still maintains its properties.

In this work, SiO_xN_y has been grown by furnace oxynitridation using the nitrous oxide (N_2O) as the precursor gas at 850^0C Films were deposited at N_2O flow of 20 and 25 ml/sec for times ranging from 45 min to 180 min. These films were characterized by ellipsometry to measure the thickness of the film and FTIR spectroscopy to study the nature of chemical bonding in the film. Metal-insulator-semiconductor capacitors (MIS-C) were fabricated to study the dielectric properties of these films.

The thickness measurement shows that the SiO_xN_y growth is occurring at a faster rate in our experiments compared to the reported results. This is an indication of probably having considerable oxygen or other impurities in the gas source. The FTIR results exhibit Si-O peaks at 1078 cm^{-1} for thin films, but we do not see a signature of Si-N peak. The 1078 cm^{-1} peak shifts by 3 cm^{-1} in thicker oxynitride to 1081 cm^{-1}, which indicates that we are preferentially incorporating nitrogen at the interface Electrical characterization of MIS-Cs shows that we have a poor dielectric with the oxide charge density in the range of $3.3x10^{16}$-$1.5x10^{19}$ cm^{-3}. Poor dielectric constant indicates lower density of the oxide and that gives a shift of Si-O mode to larger wave numbers as seen in the FTIR results. The interface-trapped charges were measured by low-frequency capacitance and conductance technique and they are in the range of 10^{12} cm^{-2} eV^{-1} at the mid-gap energy.

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Chapter 1

INTRODUCTION

1.1 Introduction:

While SiO_2 still remains the world's most used material for gate dielectrics in MOSFET, the use of SiO_2 has been questioned for sub 0.25 μm ULSI devices due to a number of problems including the impurity penetration through the SiO_2, possible reliability degradation, high gate leakage current, and need to grow ultra thin and uniform SiO_2 layers. [1] For these reasons SiO_xN_y was the first candidate to be studied to replace the pure SiO_2.[2] It exhibits superior properties compared to pure SiO_2 at ultra thin regime. Some of the important attributes of SiO_xN_y are the suppression of boron penetration and enhanced reliability.[3] As a result many research efforts have been focused to understand the growth kinetics of SiO_xN_y,[2] the role of nitrogen distribution in the films, [3] and process-property relationship.

With the decreasing size of the MOSFET devices, even thinner gate oxide will be required as discussed in Chapter 2. Therefore, the motivation for this work is to understand the reliability issues of thin (4-6 nm) SiO_xN_y for its application in next generation of devices. There is also interest in depositing these films at lower temperatures to get best diffusion barrier properties.

In order to accomplish above goals, there is need to first establish processes and characterization techniques to get device quality oxide films -this is the objective of this thesis. SiO_xN_y films were grown at 850^0C in nitrous oxide (N_2O) ambient. This temperature was chosen because in literature there are no reports of good quality films grown at this temperature. We deposited films at different flow rates of N_2O to get the optimum condition at this temperature. Films of different thickness were deposited for the same processing condition in order to understand the N incorporation in the film close to the interface and bulk.

Films were characterized by using ellipsometry and Fourier Transform Infrared Spectroscopy (FTIR). Ellipsometry data provides thickness of the oxide film. FTIR data gives information on type of chemical bonds and their surroundings. Finally, metal-insulator-semiconductor capacitors were fabricated and C-V and I-V analysis

was carried out to evaluate the dielectric properties. C-V analysis was also used to quantify the oxide defects in the SiO_xN_y. The interface trapped charged density at Si/SiO_xN_y interface was quantified using Low-frequency (Quasi-static) and Conductance method.

1.2 Thesis Outline

Chapter 2 discusses the work presently undergoing in this field and history of MOSFET scaling under the title "Literature Review". Various experiments, and their procedure have been discussed in Chapter 3, including the details about materials, equipments, and safety precautions. Results and discussion have been presented in Chapter 4 and finally conclusions in Chapter 5.

Chapter 2

LITERATURE REVIEW

2.1 Introduction:

Metal oxide semiconductor (MOS) integrated circuits now dominate the semiconductor technology, surpassing the bipolar integrated circuits in sales volume in recent years. [4] (Figure 2.1) It is now possible to have more than 10^6 transistors on a single chip the main reason behind the success of MOS IC's is it's smaller size and easier fabrication technique.

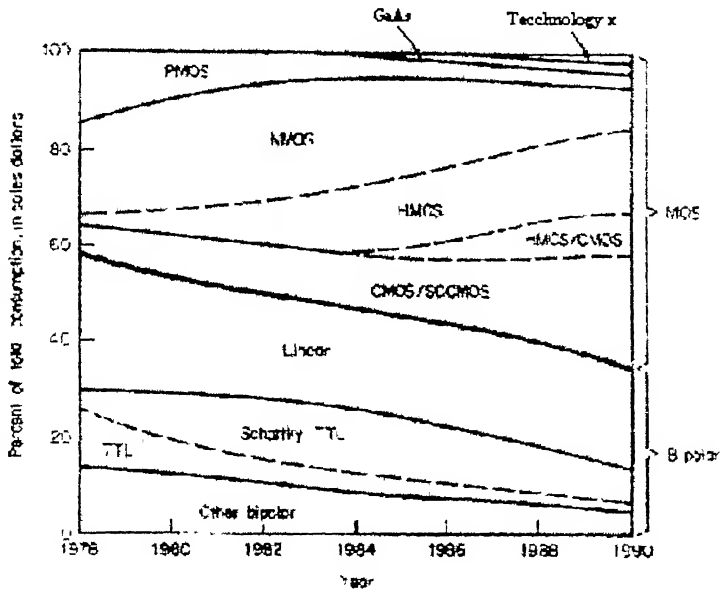


Figure 2.1 – Market Share for different semiconductor technologies [4]

To increase the device performance through shrinkage of circuit dimensions MOSFETs have been scaled down to thinner dimensions according to Moore's law [1]. The international technology roadmap for semiconductors (Table 2.1) shows that SiO_2 gate dielectrics of 1 nm or less will be required within 5 years. Since capacitance

is inversely proportional to the gate dielectric thickness, the SiO_2 layers have been scaled down to thinner dimensions. This scaling is not unlimited and beyond a certain limit i.e. for sub 0.25-micrometer ULSI devices, this scaling causes a number of problems. These are high leakages current for films below 2 nm due to direct tunnelling between gate and substrate; diffusion of boron into channel of device, charge induced damage and breakdown during device operation, device reliability.[4] Therefore, high K dielectrics are necessary to produce the required drive currents for the sub-micron devices.

Table 2.1 – MOSFET technology timetable, adopted from the international technology Roadmap for semiconductor (ITRS) [1].

First year of production	1999	2001	2002	2005	2008	2011	2014
DRAM generation	1G	1G	4G	16G	64G	256G	1T
Minimum feature size, nm	180	160	130	100	70	50	35
Equivalent oxide thickness, nm	1.9-2.5	1.5-1.9	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6

Due to its ability of improve some of the problems mentioned above, SiO_xN_y have been studied as an alternative to SiO_2. Silicon oxynitride is considered to be a modified version of pure SiO_2 containing few percentage of nitrogen. Table 2.2 compares the relevant electrical characteristics of SiO_2 While SiO_2 is grown in pure oxygen at high temperature in either furnace or RTP, oxynitrides are grown in N_2O, NO or NH_3. But the gas phase chemistry associated with these gases is quite complicated [5]. In 1990s, N_2O and NO replaced NH_3. The advantages are improved reliability, suppression of H transport and reduction of boron transport by blocking diffusion pathways.[5] Associated with these advantages are certain disadvantages like degradation of channel mobility and increased thermal budget. Therefore growing

Table 2.2 Selected properties of SiO_2 and SiO_xN_y gate dielectric layers

Properties	SiO_2	SiO_xN_y
1.Stability	Native to silicon (SiO_2 is the only stable oxide on silicon)	Not a native oxide
2. Defect Density	Low (~10^{10} $eV^{-1}cm^{-2}$ after H_2 passivation)	10^{10} - 10^{11} $eV^{-1}cm^{-2}$
3.Melting Point	1713^0C	
4.Resistivity	10^{15} ohm cm	10^{11} ohm cm
5. Dielectric Strength	10^7 V/cm	(1-2)×10^7 V/cm
6.Dielectric Constant	3.9	3.9 –7.5

2.2 Materials for post SiO_2 era:

Although many new materials with a higher dielectric constant such as Ta_2O_5, TiO_2, ZrO_2, HfO_2, $HfSiO_4$ etc have come up but they all have certain limitations with regard to material stability and integration of these dielectrics into conventional MOS process. Although no winner has emerged till now but oxynitride films provide the intermediate step in the transition to the high-k era.[6] SiO_xN_y are expected to be useful to thickness of about 1.3 nm.[1] Thinner films will exhibit excessive gate leakage current.[1] Table 2.3 is a list of requirements for alternate gate dielectrics. A comprehensive series of high-k–dielectric can be found in ref [7]. Alternative dielectric material must satisfy variety of chemical, physical, electrical and manufacturing criteria. One of the most important criteria is that gate dielectric must be thermodynamically stable on Si with respect to the formation of both SiO_2 and MSi_x.

Table 2.3. Minimum essentials for high K gate dielectric technology.

Thermodynamic stability on Si with respect to formation of SiO_2 and MSi_x
Amorphous.
$9 \leq K \leq 25$
Lower leakage than SiO_2 at t_{ox} (eq)
Low D_{it} ($\leq 5 \times 10^{10}$ $eV^{-1}cm^{-2}$)
Deposition technique should be capable of interface control (prevention of adventitious SiO_2 growth)
Conformal growth
Many other considerations (etch ability, diffusion resistance to oxygen, dopant and impurities, oxide defects, etc.)

Alternative gate dielectric must have low defect density ($< 5 \times 10^{10}$ cm^{-2} eV^{-1}) interface with Si. There are many other considerations, which must be taken into account while selecting the dielectric like etchability, oxygen diffusivity and dielectric defect structure.

Table 2.4 is a partial list of various candidates for high-k materials suggested in Figure 2.2. No simple oxide fits well on the entire criterion taken together

Table 2.4 Partial list of various candidates for high-k materials

Properties	SiO_2	Al_2O_3	ZrO_2	HfO_2	TiO_2	Ta_2O_5
Dielectric Constant	3.9	9.5	22	20	80	25
Band gap, eV	9	8.8	4	4.5	3	5
$Si + MO_x \rightarrow M + SiO_2$ at 727°C, kcal/mole of MO_x	-	63.4	42.3	47.6	7.5	-52 5
Stability of amorphous phase	High	High	Low	Low	High	Low
Silicide phase formation possible	-	No	Yes	Yes	Yes	Yes
Oxygen diffusivity at 950°C, cm^2/s	2×10^{-14}	5×10^{-25}	10^{-12}	-	10^{-13}	-

Figure 2.2 shows the elements whose oxides are stable on Si, at 1000K with respect to both SiO_2 and Silicide formation [1].

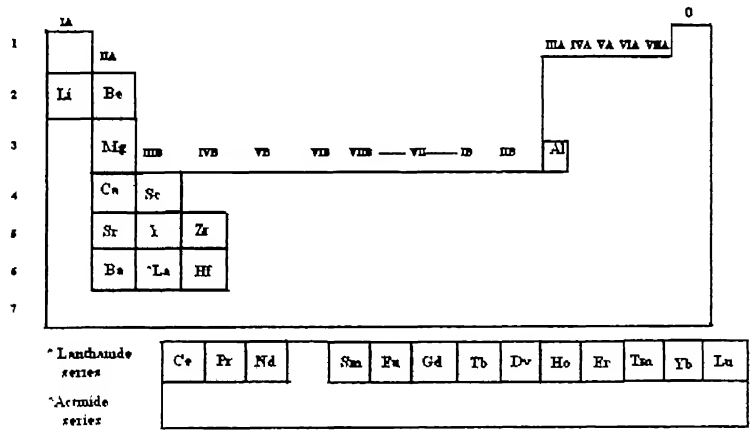


Figure 2.2 -The Elements whose oxides are stable on Si, with respect to the formation of Both SiO_2 and MSi_x at 1000 K.

2. 3 Deposition of SiO_xN_y:

SiO_xN_y layers can be grown or deposited While growth refers to thermal oxidation or oxynitridation of the Si whereas deposition usually refers to generation of the dielectric layer either chemically or physically not involving reaction with Si substrate.[1] Various techniques used for growing/ depositing SiO_xN_y are listed below:

1. Thermal Oxidation/Oxynitridation

   (a) Furnace-O_2, H_2O, O_3

   N_2O, NO, NH_3, N_2.

   (b) Rapid Thermal Processing

2. Chemical deposition

   Chemical Vapor Deposition

   Plasma Enhanced Chemical Vapor Deposition

   Jet Vapor Deposition

   Atomic Layer Deposition

3. Physical deposition

   Low energy ion implantation

   Remote Plasma nitridation

SiO_xN_y deposited by Rapid Thermal Processing may behave well with respect to electrical bulk and interface properties, but homogeneity of dielectric remains key issue. It is furnace oxynitridation that may have an edge and become important. They have good electrical characteristics and are quite uniform.[2] That is the reason for focusing on growing oxynitride in N_2O ambient using resistance heated furnace. Next, we discuss the advantages and disadvantages of different deposition techniques in brief.

2.3.1 Thermal Oxynitridation:

The main reason for success of SiO_2 is simplicity of growing thermal SiO_2 by exposing Si to O_2 at elevated temperature. Thermal growth usually takes place at higher temperature then chemical and physical deposition & this higher fabrication

temperature has been associated with improved dielectric properties.[1] The same is true for SiO_xN_y, and our attempt is to use the thermal oxynitridation at lower temperatures.

Although gate dielectrics obtained using physical & chemical deposition techniques require low temperature during deposition. They requires post deposition annealing at temperatures higher than deposition temperature to attain properties comparable to that of thermally grown oxides.[8,9] Thus overall thermal budget is not necessarily lower than the thermal grown method.

2.3.2Chemical Deposition:

This process is used mainly when lower thermal budget is the main thermal criteria. A plasma source is generally used to activate the reaction due to slow deposition kinetics at processing temperature (typically 350–600^{0}C). This technique has been used effectively to deposit ultra thin Si-O-N with precise N dissolution.[5, 9, and 10]

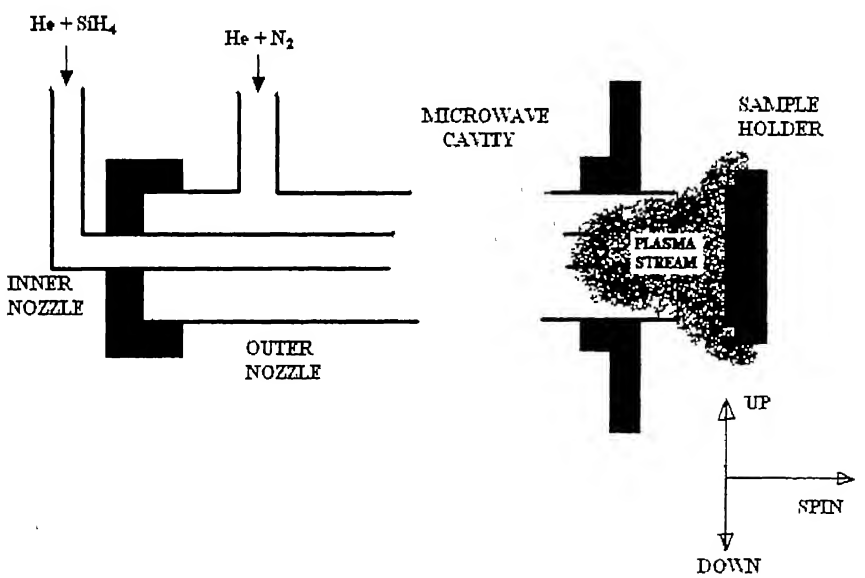


Figure 2.3 - Schematic diagram of apparatus for plasma assisted jet vapour deposition [13].

High temperature annealing (750^{0}C) is required to bring electrical performance upto the level of thermal oxides.[8, 9, 11, 12] Atomic Layer Deposition in which films are grown approximately one monolayer at a time has been used to

grow ultra thin layers (SiO_2).[1] It has the advantage of precise thickness control. Jet Vapour Deposition has been used to deposit high N containing Si-O-N.[1, 14](see Figure 2.3).

2.3.3 Physical Deposition:

Physical growth techniques for SiO_2 or Si-O-N [1] include ion implantation normally followed by annealing or oxidation. These techniques have good control over SiO_2, Si-O-N thickness, composition & structure. One can incorporate more N compared to thermal oxynitridation in ultra thin layer by using plasma nitridation. Since this technique can cause damage to the substrate, the implantation should be done at energies lower than 25 KeV.

2.4 Oxynitridation Processes:

Oxynitridation of Si i.e. oxidation of Si in N_2O [14, 15] or nitric oxide (NO) [16,17] is the most popular processing method for making SiO_xN_y films by conventional thermal routes.

2.4.1 NO oxynitridation

NO is mainly responsible for incorporation of nitrogen in both the cases.[5,16,18- 21]. Oxidation of silicon in NO results in higher N content at a given temperature compared to N_2O oxidation.[22-24] Also NO oxidized SiO_xN_y films exhibits lower leakage current & interface defects densities as well as better electrical stress properties [1, 16, 17, 23, and 25]but it may cause mobility degradation.[1]

2.4.2N_2O processing:

Oxidation of Silicon in N_2O attracts attention due to the fact that it allows for incorporation of small but significant amount of Nitrogen near Si-O-N/Si interface, but the gas phase decomposition of N_2O is complicated & people are trying to study the process property relationship by understanding the chemical kinetics of the N_2O gas phase decomposition and how reacting gas composition affect the N profile in the film. N profile in SiO_xN_y has been studied using SIMS, ellipsometry to model the whole process.[2] The key features of N_2O oxynitridation are given below

A Gas phase N_2O decomposition at high temperature

Compared to NO (a relatively stable molecule), decomposition of N_2O is rapid and complicated at high temperature. Gas flow rate, temperature, partial pressure of N_2O, reactor type and geometry all affect the kinetics and final distribution of products.[1,26]N_2O decomposes by several ways as shown (Table 2.4); the first five steps have a dominating role in N_2O decomposition to NO.[1]

B Nitrogen incorporation and removal during N_2O oxynitridation

N_2O results in less nitrogen incorporation compared to NO under similar experimental conditions.[24]The total concentration of nitrogen increases with deposition temperature as seen in Figure.2.4.[27]

Distribution of nitrogen is affected not only by the processing conditions but also by the reactor type.[16, 20, and 26] Rapid thermal N_2O films show nitrogen pile-up near the interface, while the distribution of nitrogen is broader in case of furnace grown films.[24]

While N_2O and NO both incorporate nitrogen via NO reactions the basic difference between them is that in case of N_2O, the nitrogen incorporation occurs simultaneously with nitrogen removal from the upper layers of the film.[19 Competition between nitrogen incorporation and nitrogen removal influences the final distribution and concentration. Due to the difference in reactivities of NO, N_2O and O_2 with Si, SiO_2 and SiO_xN_y, properly chosen sequences of thermal reactions can lead to SiO_xN_y films with varying nitrogen concentrations and profiles, and therefore different electrical properties

Table 2.5 – Reaction scheme for N_2O decomposition.[1]

1. $N_2O \rightarrow N_2 + O$
2. $N_2O + O \rightarrow NO + NO$
3. $N_2O + O \rightarrow N_2 + O_2$
4. $O + O \rightarrow O_2$
5. $NO + O \rightarrow NO_2$
6. $NO_2 + O \rightarrow NO + 2O$
7. $NO_2 + NO_2 \rightarrow NO + NO + O_2$
8. $NO_2 \rightarrow NO + O$
9. $NO_2 + NO_2 \rightarrow NO_3 + NO$
10. $NO_3 + NO \rightarrow NO_2 + NO_2$
11. $NO_2 + O \rightarrow NO_3$
12. $NO_3 \rightarrow NO + O_2$
13. $NO_3 + O \rightarrow O_2 + NO_2$
14. $NO_2 + NO_2 \rightarrow N_2O_4$
15. $N_2O_4 \rightarrow NO_2 + NO_2$
16. $NO_2 + NO_3 \rightarrow N_2O_5$
17. $N_2O_5 \rightarrow NO_2 + NO_3$
18. $O_2 + O \rightarrow O_3$
19. $O_3 \rightarrow O_2 + O$
20. $O_3 + O \rightarrow O_2 + O_2$
21. $O_3 + NO \rightarrow NO_2 + O_2$

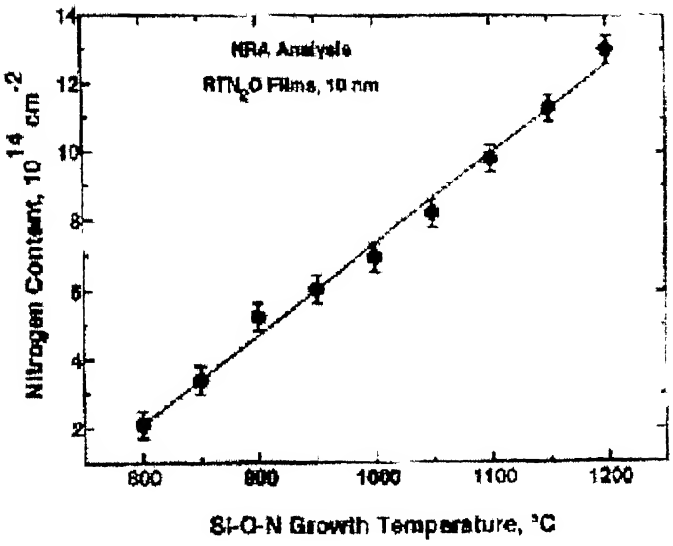


Figure 2.4 - Nitrogen content of 10nm Si-O-N films grown in N_2O by rapid thermal oxidation at 1000°C as measured by nuclear reaction analysis

2.5 Nitridation in NH_3

Nitridation in NH_3 was one of the first methods to incorporate nitrogen in SiO_2 films.[1] Nitrogen piles up at the interface as well as the outer surface during the earlier stages of nitridation. Concentration of nitrogen increases slowly with nitridation time and also uniformity is improved.[1] Ammonia nitridation causes high concentration of hydrogen into SiO_2 film, which can act as electron traps. SIMS study shows that hydrogen concentration increases with time and temperature. Hydrogen piles up mostly near the interface.[1] It has been found that post nitridation anneal in hydrogen free atmosphere can reduce the concentration of hydrogen. Due to the ill effects of hydrogen on device performance, it is generally preferred to have lower nitridation temperature and shorter times, because it ensures lesser hydrogen introduction at the interface. Researchers have carried out detailed study to investigate the behaviour of hydrogen, oxygen and nitrogen in NH_3 nitrided SiO_2.[1]

2.6 Nitridation in N_2

Although nitrogen is relatively inert but annealing of SiO_2 films in nitrogen results in initial reduction of fixed oxide charge.[1] This has been attributed to the formation of Si-O-N layer near the interface detected by XPS study.[1]

2.7 Si/SiO_xN_y system:

In this section, some of the properties that make SiO_xN_y an excellent gate oxide candidate for next generation of MOSFET devices are discussed

2.7.1 Diffusion Barrier Properties:

Boron penetration in the gate oxide causes threshold voltage shifts & degrades reliability.[1, 28] One of the important property of silicon oxynitride is its ability to act as a barrier to impurities mainly by blocking diffusion pathways notably for Boron [1, 29].

A model has been proposed to explain the "stopping power" of nitrogen in SiO_xN_y.[1] According to this model, the role of nitrogen is to compete with B for occupation of the defects sites. Another model has also been suggested which assumes that boron diffuses substitutionally for Si atoms.[1] The role of Si-N bond is to impede substitution for that Si atom.

2.7.2 Enhanced Reliability:

The n- and p-channel MOSFET's using SiO_xN_y as gate oxide, have improved performance and reliability. Both n- and p- channel MOSFET's show excellent immunity to channel hot carrier degradation. The improvement in hot carrier reliability is attributed to the efficient incorporation of nitrogen in the dielectric.

2.7.3 Oxide defects and interface defects

The dielectric properties of SiO_xN_y have been studied using CV and conductance methods. Typical curves are obtained in case of oxynitride using the PECVD technique and the value of dielectric constant using the capacitance in accumulation region has been found to be 5.5.[30] The density of defect states has been calculated by low frequency capacitance method, and it is of the order $6\text{-}7\times10^{11}$ cm^{-2} eV^{-1}, which were confirmed using the DLTS tests.[30]

It has been observed that the NO annealed SiO_2 have excellent initial characteristics and interface trap density D_{it} values are in the 10^{10} eV^{-1} cm^{-2} range.[23] This value changes with the NO anneal time, the increase being significantly small. The D_{itm} (mid gap interface density) values are 1.5×10^{10}, 1.8×10^{10}, and 2.5×10^{10} cm^{-2} eV^{-1} corresponding to the 10, 20 and 80 sec anneals. It is believed that nitrogen incorporation at the SiO_2/Si interface is responsible for this increase in initial D_{itm}. [9]

In another study C-V measurements have been carried out to characterize the $Si_xO_yN_z$ films deposited by chemical vapor deposition and the value of dielectric constant has been found to be lying between 5.5 to 6.0 at 100 KHz for different film thickness.[31]

CHAPTER 3

EXPERIMENTAL WORK

This chapter consists of three sections. In the first section of the chapter the materials, sample details and equipments used in the study are introduced in brief. The second section gives details of the processing procedure used to grow SiO_xN_y. The last section of the chapter gives details of the analysis used for the characterization

3.1 MATERIALS AND EQUIPMENTS:

3.1.1 Substrates:

The SiO_xN_y films were grown on p-type silicon having thickness 250–300 μm. The resistivity of the substrate is 1-2 Ω cm. The orientation of the substrate is (100). The dimension of the wafer used in our experiments is about 1cm x 2cm.

3.1.2 Gases and Chemicals

The gases used for oxynitridation are nitrogen and nitrous oxide. Nitrous oxide was used mainly for oxidation purpose while nitrogen was used for the purpose of pre and post oxidation annealing of the oxynitride and post metallization annealing of the MIS devices

3.1.3 Furnace:

We have used the resistance heated horizontal tube furnace of quartz (60-cm long) for oxynitridation. The outer diameter of the furnace is 5.1 cm and inner diameter is 4.6 cm. The thermocouple used was of Platinum-Rhodium. The furnace is connected to a temperature controller through which we can set the desired temperature.

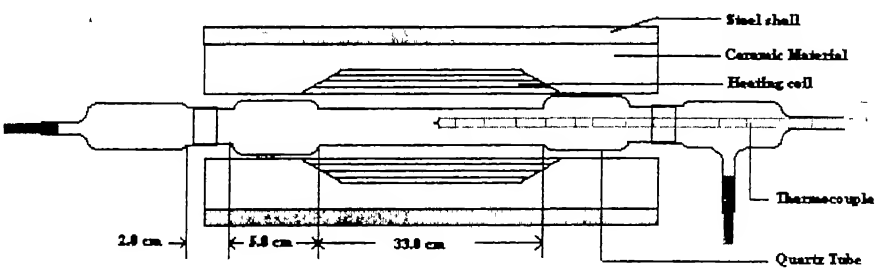


Figure 3.1 – Schematic diagram of the furnace used

3.1.4 C-V Instrument:

The C-V instrument used for the analysis of devices is Agilent's 4294A Impedance analyser. The frequency range of this instrument is from 40 Hz to 110 Mhz. The DC bias voltage range is –40 to +40 volts. We have different types of sweeps and measurement on this instrument. We can sweep the impedance as a function of frequency, DC bias voltage and oscillator signal level. The operating details are given in Appendix A

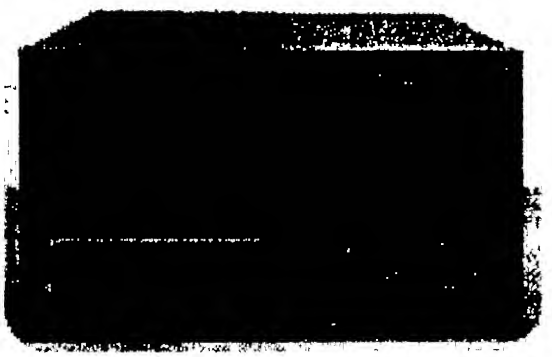
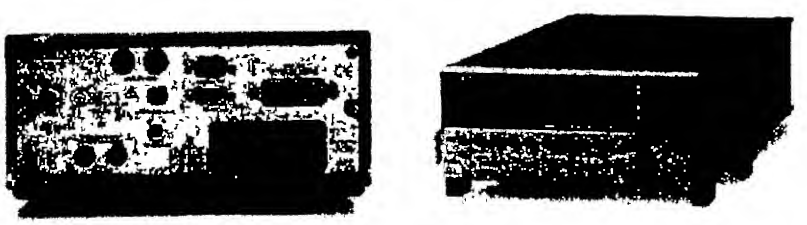


Figure 3.2 – Agilent's 4294A Impedance analyser (Front view).

3.1.5 I-V Instrument:

The I-V instrument used for the analysis of device is Keithley's model no 6172. We can measure the current as function of applied voltage across the device in various ranges eg nano ampere pico ampere etc. Also it can measure the resistivity, leakage current of capacitor, resistance and much more with good accuracy. The operating details are given in Appendix A



Rear View Main View

Figure 3.3 - Keithley's model no 6172

3.2 OXYNITRIDATION PROCEDURE:

3.2.1 Organic cleaning:

The silicon wafers were first degreased with a mild soap solution and then thoroughly cleaned with organic solvents viz, trichloroethylene, acetone and methanol in succession, finally cleaned in the de-ionised water and dried using nitrogen gun.

3.2.2 RCA Cleaning:

After organic cleaning standard RCA cleaning was performed having following steps [4]

Step 1: The silicon wafers were heated at a temperature of 80-90°C for about 10 minutes in a solution of de-ionised water (DI water), hydrogen peroxide (H_2O_2), and ammonia solution (NH_3) (Volume ratio being 5:1:1). Then rinsed in DI water.

Step 2: The wafers were subsequently etched in dilute HF acid (HF: DI 1:100) for 10 minutes. Then washed in DI water 5-6 times.

Step 3:The wafers were heated again at a temperature of 80-90°C for 10 minutes in yet another solution of DI water, hydrogen peroxide and hydrochloric acid in volume ratio of 6:1:1 and rinsed thereafter in DI water for 5-6 times.

Step 4: The cleaned wafers at this stage were etched in diluted HF acid (ratio 1:20) for 1 minute. Finally, wafers were washed in DI water and dried using nitrogen gas.

3.2.3 Oxynitridation:

Before staring the oxynitridation all gas lines were purged with the nitrogen gas. Wafers were transferred to the conventional resistance heated furnace at a stand by temperature of 700°C. Temperature ramp up to oxidation temperature was done in pure N_2. Oxynitridation was performed in pure nitrous oxide ambient at a temperature of 850°C. Oxynitridation has been carried out for conditions shown as crosses in the Table 3.1 These samples are referred as A1, A2, A3 and A4 in the rest of the thesis After the oxidation of silicon in nitrous oxide, post deposition annealing was done in nitrogen only for about 15 minutes and then the sample was allowed to cool up to 700°C before taking it out.

Figure 3.4 gives the flow chart of the procedure followed for the oxidation.

Table 3.1 Processing Conditions for which oxynitridation was carried at 850° C

Flow rate	Time			
	45 min	120 min	150 min	180 min
20 ml/sec	X (A4)			X (A1)
25 ml/sec		X (A3)	X (A2)	

Safety Precautions:

Since nitrous oxide (N_2O), laughing gas is used for the anaesthetic applications we took special precautions for using the nitrous oxide. The pipeline arrangements were made for taking the exhaust of the N_2O outside the lab.

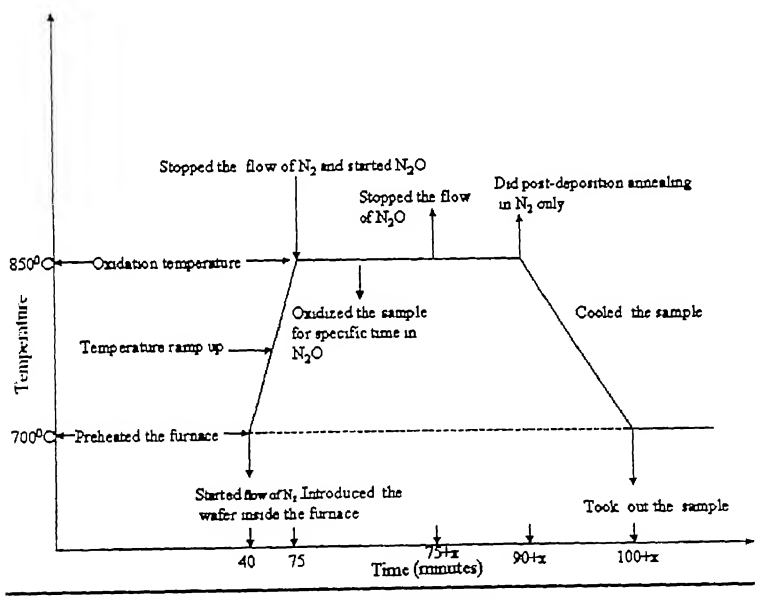


Figure 3.4 Process chart for the growth of silicon oxynitrde

3.2.4 Backend Processing

During thermal oxidation in N_2O environment, oxynitride was grown on the both sides of silicon wafers, which is undesirable. In order to remove the oxynitride at the back side of the sample, dilute HF acid (HF: DI 1:10) was used. In order to protect the front section, a cotton swab was used to remove the oxynitride from the backside

3.2.5 Capacitor fabrication:

Metal-insulator-semiconductor capacitors (MIS-C) were fabricated after measurement of the SiO_xN_y thickness using ellipsometry. Aluminium was used as the metal for deposition as a gate material. Aluminium was deposited at the backside i.e the end having no oxide using the blanket evaporation unit. The front side was deposited with mask of brass having dots of 1.0mm and gap between dots of 1 mm.

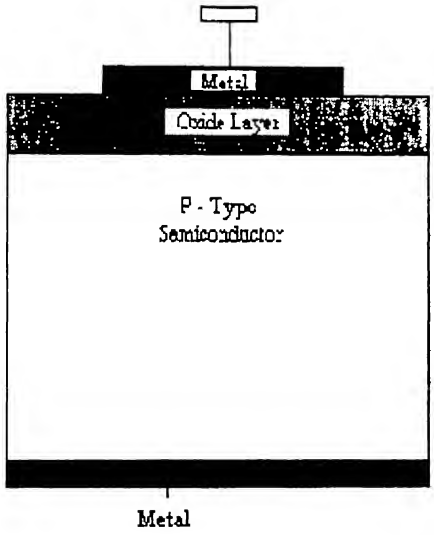


Figure 3.5 – Typical MIS-C structure.

3.2.6 Device Annealing:

After capacitors were fabricated using the mask they were annealed in nitrogen atmosphere at 250^0C for one hour [4]. Annealing was done to improve aluminium contacts.

3.3 Optical and Electrical Characterization: -

3.3.1 Ellipsometry

Ellipsometry is based on the measurement and subsequent modeling of changes in the polarization state of a light beam reflected (Figure 3.6) from a sample surface. The measured parameters are the ellipsometric angles ψ and Δ, defined from the ratio of the Fresnel Reflection coefficient R_{II} and R_I for the light polarized parallel and perpendicular to the plane of incidence.

$$R_{II}/R_{I} = \tan(\psi) \exp(i\Delta)$$

The reflection coefficients are determined by the optical properties and composition of the substrate and over layers, their thickness, and morphology. The parameters ψ and Δ can be measured either at a given wave length of light i.e. single wavelength ellipsometry (most often 633 nm) or as a function of photon energy i.e. spectroscopic ellipsometry. The single wavelength configuration is often used for fast, nondestructive online monitoring of film thickness, provided refractive index of the film is known. The spectroscopic mode allows determination of the refractive index (η) as well as the thickness.

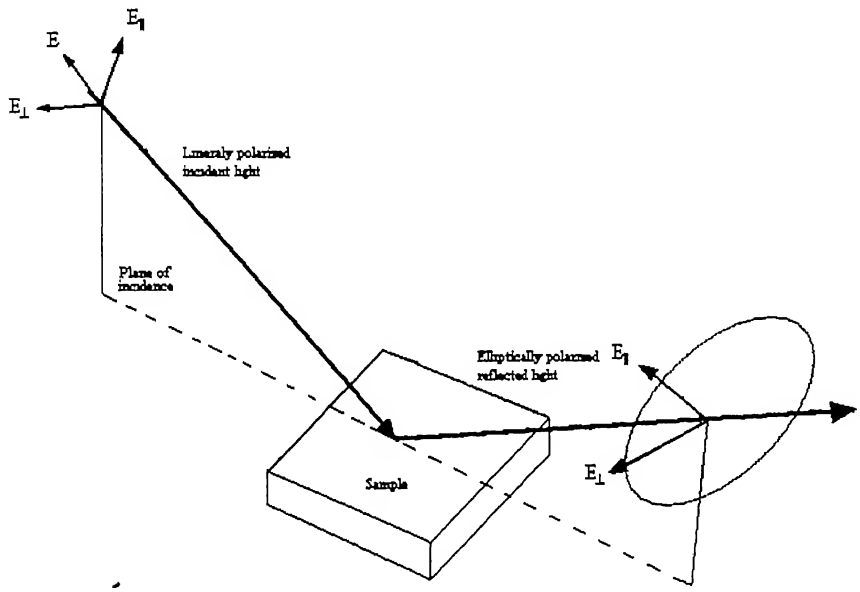


Figure 3.6 - Principles of an ellipsometric measurement

3.3.2 C-V measurements

The most important measurement in a MIS-C device is to measure capacitance as a function of DC gate bias. This is known as CV (capacitance-voltage) plot [4]. Its importance is due to the fact that one can extract informations like dielectric constant, flat band voltage, oxide thickness, and density of defect states in the oxide.

A typical test structure and set up is shown in Figure 3.7. The test structure consists of a gate electrode (usually metal in dot form) over a gate oxide. This forms a simple MIS-C device. The capacitance meter measures the capacitance of the structure while applying the dc bias.

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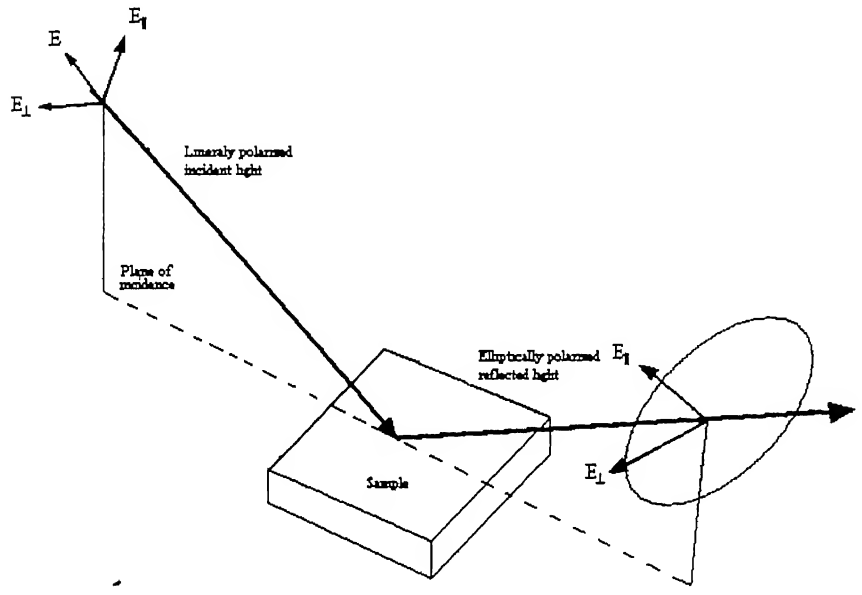

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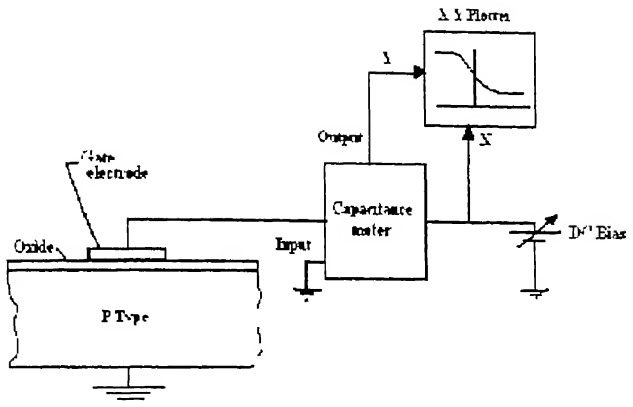


Figure 3.7 C-V Plot test structure and set up

Capacitance – voltage measurements were performed on MIS-C capacitors using an Agilent's 4294A precision impedance analyser (40 Hz-110 MHz). Prior to any data acquisition, an open and/or short circuit correction was performed. A three-element model consisting of a capacitance, C, a conductance, G, and series resistance Rs, as shown in Figure 3.8 (a), can approximate the MIS capacitor. For all the measurements made, the impedance analyser assumes that the device under test (DUT) is represented by a capacitance, C_P, and conductance, G_P in parallel or a capacitance, C_S, and resistance, R_S in series, as shown in Figure 3.8 (b) and (c). The procedures followed to calculate the dielectric constant, oxide defects, and density of defects states D_{it} are described next.

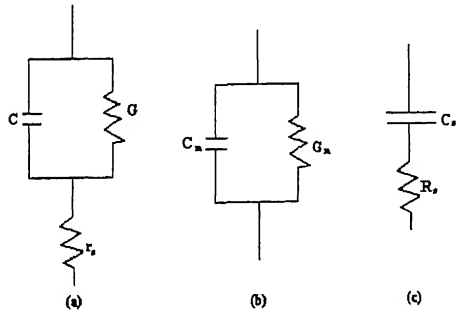


Figure 3.8-Equivalent circuits for capacitance –voltage measurement; (a) 3-element model, (b) parallel equivalent circuit, and (c) series equivalent circuit for MIS capacitor

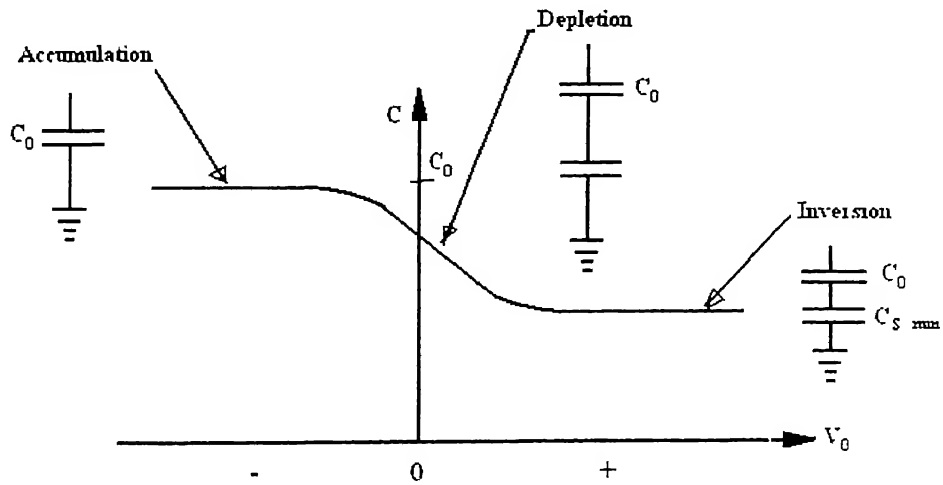
3.3.2.1 High Frequency CV

Capacitance meters measure capacitance by applying a small, typically 10-50 mV, ac voltage on the top of a dc bias. When a relatively high frequency signal is used, usually 1MHz, the resulting CV plot is given in Figure 3.9. This is by far the most commonly used type of CV plot for analysis. With a negative bias, p-type silicon is in accumulation; the capacitance is that of a parallel plate capacitor with oxide as the dielectric. The oxide capacitance in this region is given by

$$C_o = \frac{\varepsilon_r \varepsilon_o}{d} \qquad [3.1]$$

Where C_o is the capacitance per unit area in the accumulation region, permittivity of the vacuum ε_0 is 8.86 x 10^{-14} F/cm, and ε_r is the relative permittivity of oxide. This is how dielectric constant of the SiO_xN_y was calculated in this work; the value of film thickness was taken from ellipsometry measurement.

At a gate voltage that is more positive than flat band voltage V_{FB}, a depletion region is formed in the semiconductor. This creates a capacitor, C_S, in series with the oxide capacitor and produces a drop in total capacitance. When the gate voltage reaches and exceeds the threshold voltage V_T, a layer of inversion charge is formed. Then if the gate voltage is further increased, the inversion layer increases its charge to balance the gate and the depletion layer does not widen further.



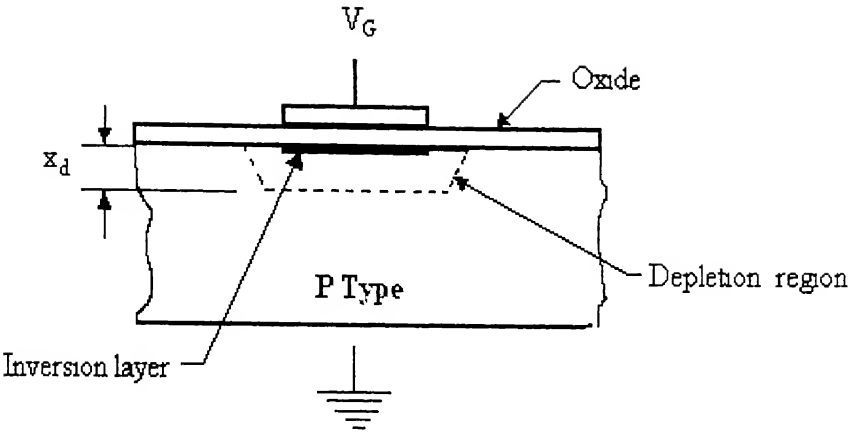


Figure 3.9 - Typical C-V Plot (High frequency) for p-Type substrate

3.3.2.2 Low frequency C-V Plot

When the test frequency of the capacitance is very low, the C-V plot looks like Figure 3.10. Just as in case of high frequency, the capacitance starts out at maximum at accumulation and drops in depletion. The high frequency and low frequency C-V plots are identical in accumulation, depletion and most of weak inversion for an ideal MIS-C. The difference comes in strong inversion, where the surface potential on the semiconductor, Φ_S, is equal to twice the potential difference between the E_F of the doped semiconductor (substrate) and the intrinsic Fermi level E_i. This is known as the threshold voltage to create inversion layer. It should be pointed out that threshold voltage does not correspond to the minimum capacitance but is slightly shifted beyond that as shown in Figure 3.10. The difference in the low and high frequency curves in the inversion region comes from the fact that minority carriers are not generated fast enough to follow the high frequency AC signal

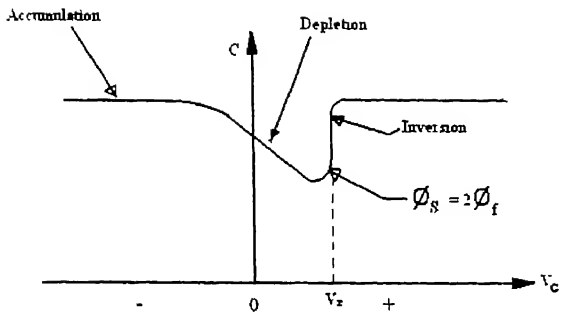


Figure 3.10 - Typical low frequency C-V plot

3.3.2.3 **Estimation of oxide charges**

The curves in Fig 3.9 and 3.10 are calculated for an ideal MIS Capacitor with no oxide charges. By comparing the ideal C-V curve with the experimental C-V curves we can estimate different oxide charges. Typically there are four kinds of oxide charges (i) fixed oxide charge (Q_f) (ii) oxide trapped charges (Q_{ot}) (iii) mobile ionic charge (Q_m) and (iv) interface trapped charge (Q_{it}). Nature and effect of the oxide charge on MIS-C characteristic are discussed in detail in ref [41]. Here, we are interested in how to estimate these charges in the SiO_xN_y films grown by us.

The technique we are using in this work estimates oxide charge Q_{ox} where $Q_{ox} = Q_f + Q_{ot} + Q_m$) all together, we cannot distinguish among them. But we are able to estimate interface-trapped charges, which is a good indicator of the interface quality between the oxide and semiconductor.

3.3.2.4 **Oxide charges**

In order to estimate the total oxide charge, Q_{ox}, first we estimate the quilibrium hole concentration in the substrate based on the resitivity of the sample, vhich is 10^{16} cm^{-3} We know the oxide thickness from ellipsometry, which was stimated using refractive index of 1.46 (refractive index of SiO_2). In other words, this s an equivalent SiO_2 thickness of SiO_xN_y film. Now using Fig 3.11 we can find out lat –band capacitance of the ideal MIS-C structure.

Now from the measured C-V curve we know the voltage at C_{FB} and we know that for an ideal MIS-C structure without oxide charge it should be zero. This gives us a measure of ΔV_{FB} which can be used to estimate total oxide charge using the following the equations:

$$\Delta V_{FB} = \Phi_m - \frac{Q_{ox}}{Co} \qquad [3\ 2]$$

Where C_o is the capacitance per unit area of the oxide and Φ_m is given by the following equation

$$\Phi_{ms} = \Phi_m - \left[\chi + \frac{E_g}{2} + \varphi_B \right] \qquad [3.3]$$

Where Φ_{ms} is metal-semiconductor work function difference, Φ_m is metal work function (V); χ is substrate material work function (electron affinity)(V), E_g is the substrate material band gap (V), and Ψ_B is the bulk potential (V).

By dividing this by the charge, we get the number of oxide defects per unit area, $N_{ox} = \frac{Q_{ox}}{q}$. Since we know the oxide thickness, we convert the number of oxide defects per unit area in a MIS-C device to number of defects per unit volume of the insulator, in this case SiO_xN_y by dividing by the thickness

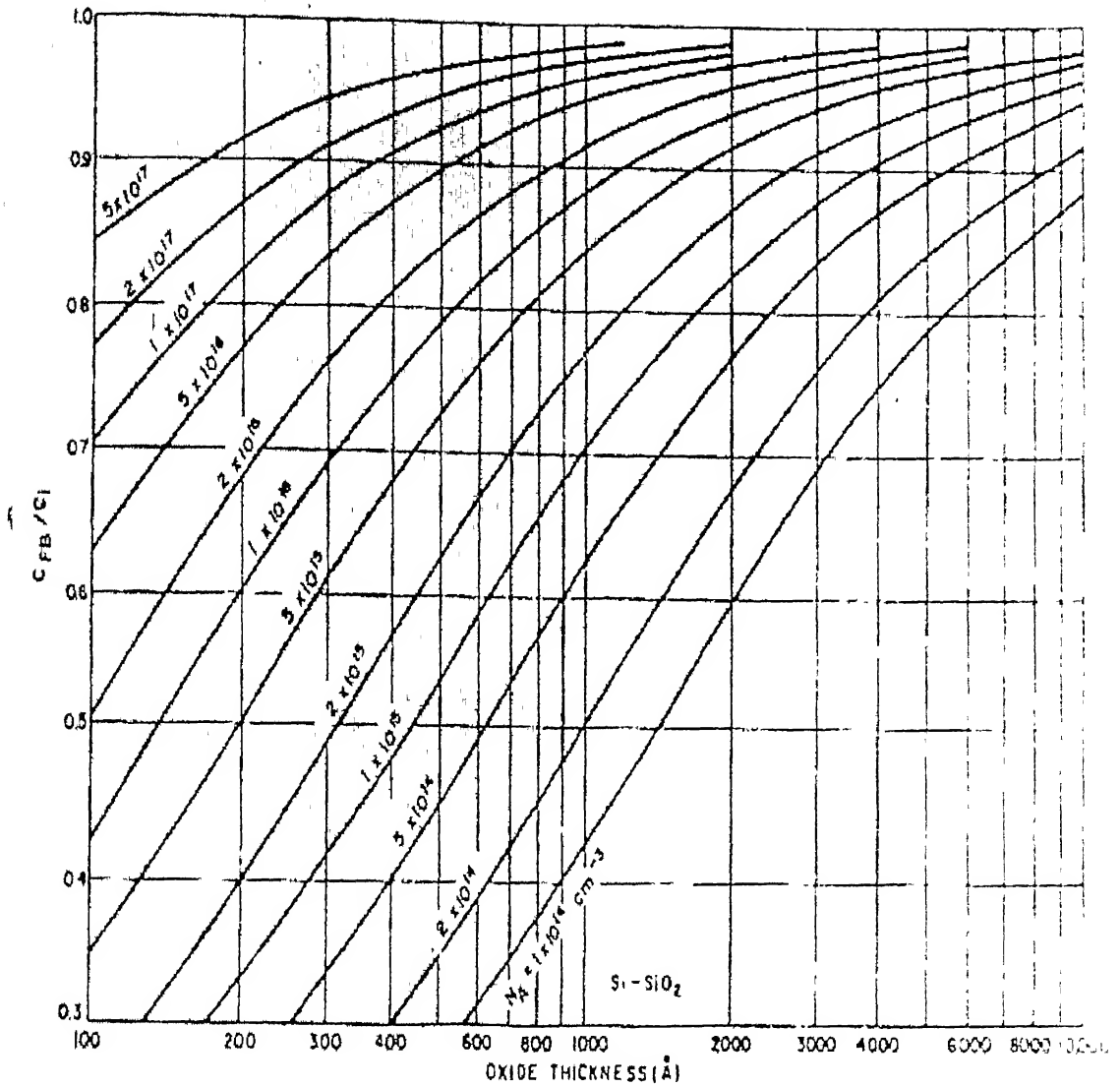


Figure 3.11 Normalized flat-band capacitance versus oxide thickness with doping as the parameter for ideal MIS diodes. (After Sze.Ref .42.)

3.3.2.5 Interface trapped Charge

The interface-trapped charge, D_{it}, exist due to broken bonds at oxide/semiconductor interface. They give rise to electronic states in the forbidden gap of the semiconductor. These days it is routine to get very low values of D_{it} in the range of 10^{10} $cm^{-2}eV^{-1}$ for Si/SiO_2 interface. A number of methods have been developed over the years, but we are using the Low-Frequency (Quasi-static) and Conductance method to calculate the D_{it}. A good overview of the nature of interface trapped charge and methods for its characterization can be found in ref [32].

3.3.2.6 Low-Frequency (Quasi-static) Method

This is relatively simple method and has become one of the most common interface trapped charge measurement methods. It provides information only on interface trapped charge density, but not on the capture cross section of the traps. Berglund developed the basic theory behind the qausistatic method [33]. The method employs the comparison between low-frequency C-V curves with one free of interface trap effects. The latter can be a theoretical curve but generally HF C-V curve is taken at a frequency where interface traps are assumed to not to respond. The LF capacitance is given by:

$$C_{LF} = \frac{1}{\left(1/C_{ox}\right) + 1/\left(C_S + C_{it}\right)} \qquad [3.4]$$

Where C_o is oxide capacitance, C_S is semiconductor capacitance and C_{it} is related to interface trap density by

$$D_{it} = \frac{C_{it}}{q} \qquad [3.5]$$

$$\text{Giving} \quad D_{it} = \frac{1}{q}\left(\frac{C_o C_{LF}}{C_o - C_{LF}} - C_S\right) \qquad [3.6]$$

The determination of D_{it} from Equations [3.5] is quite time consuming and a simplified approach was proposed by Castagne and Vapaille [33]. It eliminates the

uncertainty associated with measured C_S in equation in [3.3] and replaces it with a measured C_S, from the HF C-V curve which we can find from the equation:

$$C_S = \frac{C_o C_{HF}}{C_o - C_{HF}} \qquad [3.7]$$

Finally we can calculate D_{it} as follows

$$D_{it} = \frac{C_o}{q}\left(\frac{C_{LF}/C_o}{1-C_{LF}/C_o} - \frac{C_{HF}/C_o}{1-C_{HF}/C_o}\right) \qquad [3.8]$$

The Eq 3.8 is used to calculate D_{it} as a function of gate voltage. We convert the gate voltage into the energy for the trap states using the following equation:

$$\Psi_s(V) - \Psi_b = \int_{V_{FB}}^{V}\left(1-\frac{C_{LF}}{C_o}\right)dV \qquad [3.9]$$

Where Ψ_s (V) is the surface potential at the interface as function of the gate voltage. At $V=V_{FB}$ the surface potential is equal to Ψ_b. Hence, our reference point in the bandgap for zero energy will be at flat band voltage, which we have calculated earlier. Finally we plot D_{it} as a function of the energy in the band gap as calculated using the above equation.

3.3.2.7 Extraction of D_{it} from Conductance Measurement

Nicollian and Goetzberger first proposed the conductance method in 1967 and it is generally considered to be the most sensitive method to determine D_{it} [33]. Interface trap densities of 10^9 cm^{-2} eV^{-1} and lower can be measured. It is the most complete method because it yields D_{it} in the depletion and weak inversion regions of the band gap, the capture cross sections for the majority carriers, and information about surface potential fluctuations. It is based on the measurement of equivalent parallel conductance G_P of MIS-C capacitor as a function of bias and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of MIS-Capacitor appropriate for the conductance method is shown in Figure 3.11. It consists of oxide capacitance C_o, the semiconductor capacitance C_S, and the interface trap capacitance C_{it}. The capture and emission of carriers from the D_{it} is a lossy process, represented by the resistance R_{it}. For interface trap analysis it is convenient to replace the circuit of Figure a by Figure b where C_P and G_P are from a simple circuit conversion

$$C_p = C_S + \frac{C_{it}}{1+\left(\omega\tau_{it}\right)^2} \qquad [3.10]$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad [3.11]$$

Where $C_{it} = qD_{it}$, $\omega = 2\pi f$ (measurement frequency), and $\tau_{it} = R_{it}\ C_{it}$, G_P is divided by ω to make the equation symmetrical in ωit. Equations 3.10 and 3.11 for interface traps with a single energy level in the band gap. Interface traps at the Si-SiO_2 interface, however, are located within a few kT/q above and below the Fermi level for such a continuum of interface traps. This results in time constant dispersion and gives the normalized conductance as [33]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln\left(1+\omega^2\tau_{it}{}^2\right) \qquad [3.12]$$

Equations 3.10 and 3.11 shows that the conductance is easier to interpret than the capacitance because C_S is not required in equation 3.11.The conductance is measured as a function of frequency and plotted as G_P/ω versus f .The function G_P/ω has a maximum at $\omega = 1/\tau_{it}$, and at that maximum $D_{it} = 2G_P/q\ \omega$. For equation 3.12 $\omega = 2/\tau_{it}$, and $D_{it} = 2.5G_P/q\ \omega$ at the maximum. Hence we determine D_{it} from the maximum G_P/ω. Capacitance metres generally assume the device to consist of parallel $C_m - G_m$ combination as shown in Figure 3.12.This is how we get another

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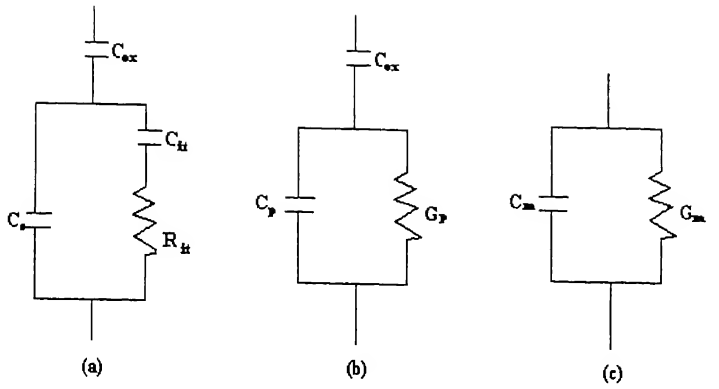


Figure 3.12 Equivalent circuits for conductance measurements;(a) MIS-C capacitor with interface trap time constant $\tau_{it}=R_{it}.C_{it}$, (b) simplified circuit of (a), (c) measured circuit

3.3.3 I-V Measurements

Current –Voltage measurements were done using the Keithley's model no 6172. Since the keithley's 6172 have the ability to simultaneously apply a voltage (current) while measuring the current (voltage), the leakage current can be measured through the gate dielectric. Gate leakage current is one of the important criteria to characterize the gate dielectric. Current voltage measurement at different temperatures can be used to study the conduction mechanism.

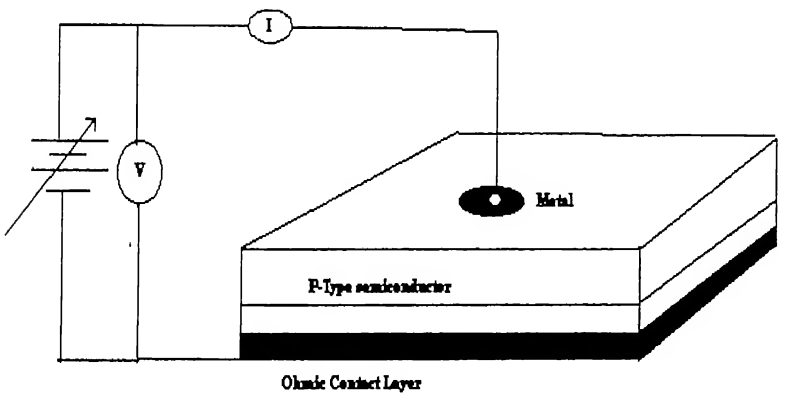


Figure 3.13 I-V Connection

3.3.4 FTIR Measurements:

FTIR stands for Fourier Transform Infra Red (IR), infrared spectroscopy, in this technique, IR radiation is passed through a sample. Some of the infrared radiation is absorbed by the sample and rest is transmitted. The resulting spectrum represents the molecular absorption, creating a molecular fingerprint of the sample. This information is used to understand the nature of chemical bonds in the samples.

CHAPTER 4

Results and Discussion

In this chapter, the results of electrical and structural characterization of SiO_xN_y films, grown by oxidation in N_2O at 850^0C, are discussed We have already presented the growth conditions and analysis procedure in the last chapter.

4.1 Dielectric properties of SiO_xN_y

Table 4 1 summarizes the results of ellipsometry and high frequency C-V measurements for different samples The thickness of SiO_xN_y was estimated from ellipsometry measurements assuming refractive index of 1.46 as done by other researchers.[34,35] The thickness measured are found to be higher than what was estimated from similar experiments in the literature at 950^0C.[2,36] This points to possible presence of oxygen and water vapor in the N_2O gas source.

The dielectric constant and oxide charges were measured from high frequency C-V curve, a typical curve is shown in Fig. 4.1 for sample A2. The arrow indicates the direction of the voltage sweep during measurement. C-V curves from other samples are given in Appendix B.The value of dielectric constant is very low as calculated from the accumulation region of the C-V curve for all the samples, which is an anomaly. It is impossible to get dielectric constant values <1 which is the value for air. Given the high density of oxide charges in the films we expect to get lower value of dielectric constant, but not so low. Introducing impurities like carbon and fluorine in SiO_2, or by making SiO_2 porous is a common way to reduce the dielectric constant of the film. [37-39]

The lowest dielectric constant obtained by researchers is 1.7 for porous silica film. Later we show that based on FTIR results that we are growing an oxynitride with very little N incorporation. We also find evidence that oxynitride film has dielectric constant closer to that of SiO_2. It is strongly suspected that some feature of our device preparation or measurement set-up is giving this problem with the absolute measurement of the capacitance. This needs to be rectified for future work.

In spite of the problem with the absolute measurement of dielectric constant, the defect characterization can be still done as normalized values of capacitance, C/Co, are used in these calculations. Moreover, the calculations of interface defect densities are confirmed by two different methods, and were found to be in good agreement. The oxide charges in a gate oxide are normally 2-3 orders of magnitude lower than the values seen in these samples (Table 4.1). This can be further improved with better procedures for cleaning the substrate and processing gases. The current work was done with gases obtained locally and there were no purifiers in the gas line.

Table No 4.1 Film thickness, dielectric constant and density of oxide charge

Sample No	N_2O flow rate (ml/sec)	Time (Minutes)	Thickness (Angstrom)	V_{FB} (Volts)	Density of oxide charges (Cm^{-3})	Dielectric Constant
A1	20	180	339	-18.58	3.48E17	0.55
A2	25	150	160	-2.49	6.56E16	0.26
A3	25	120	589	-33.74	3.76E17	0.97
A4	20	45	40	-23.16	1.58E19	0.28

In Table 4.1, dependence of film thickness on oxidation time is not systematic at all. Sample A2 has thinner oxide growth compared to A3, although it was oxidized for longer time. This seems to be an indication of poor control of gas quality during processing.

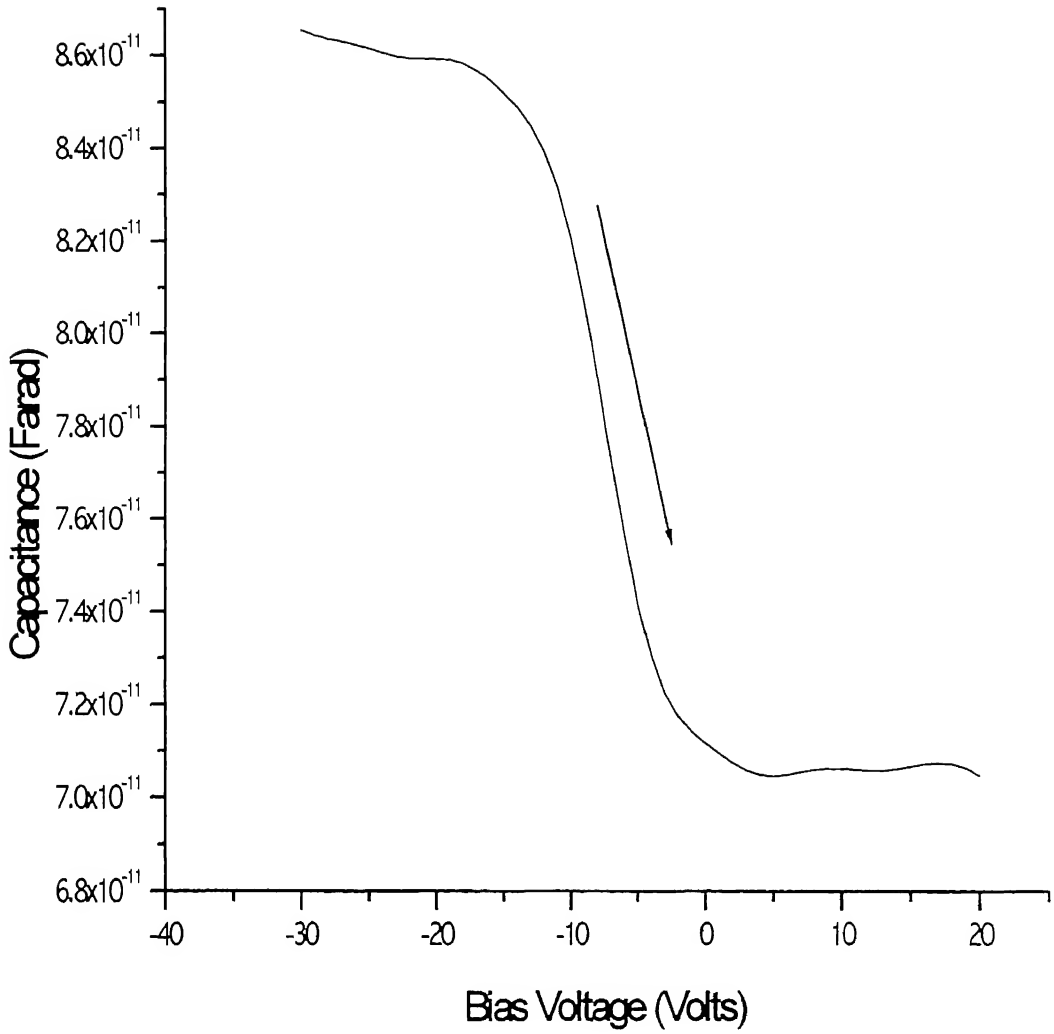


Figure 4.1 C-V plot for sample A2 (Silicon Oxynitride oxidized for 180 minutes in N_2O at flow rate of 20ml/sec) at 1 MHz.

4.2 Hysteresis in the HF C-V curves

It was shown in the last section, that the SiO_xN_y films grown had a high density of oxide charges Another indication of the oxide charges is the voltage and sweep direction dependent C-V curves This indicates there is electron trapping occurring at the defect sites in the oxide. Hysteresis effect is shown in Fig 4.2 and there is some memory effect in devices as we change the sequence of measurement as seen in Fig. 4 3.

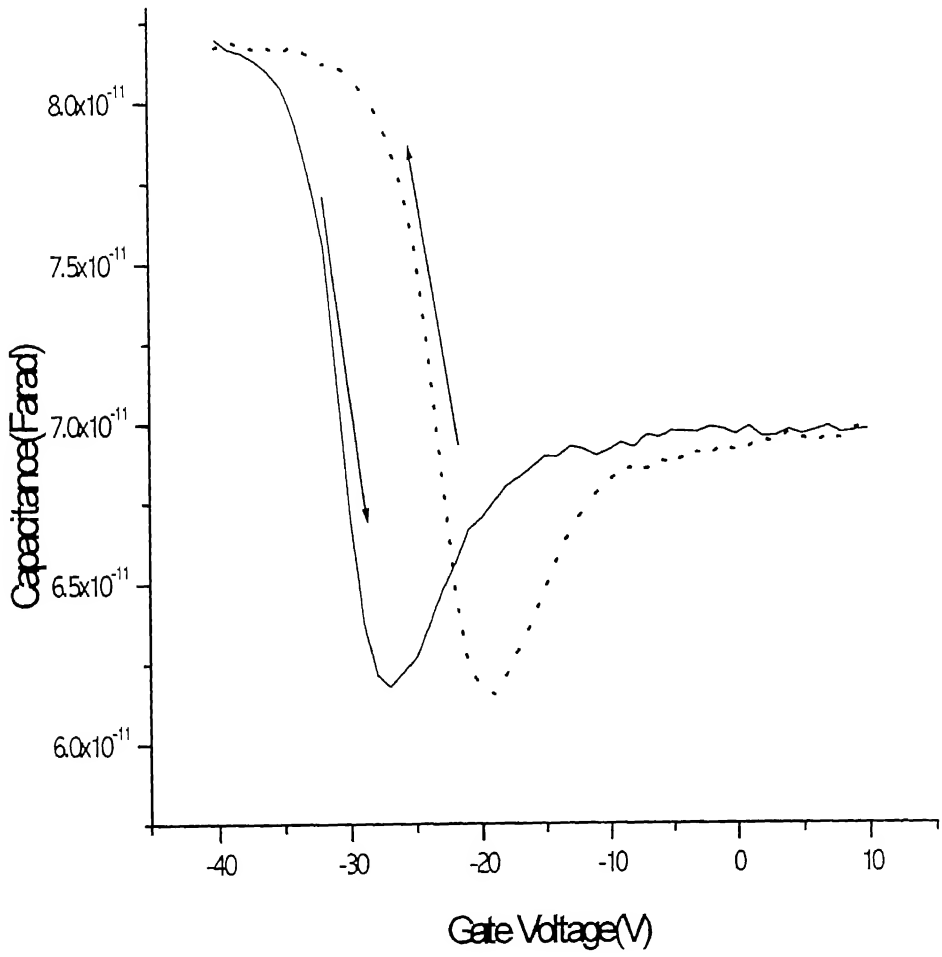


Figure 4.2 Effect of Sweep directions on the C-V plot

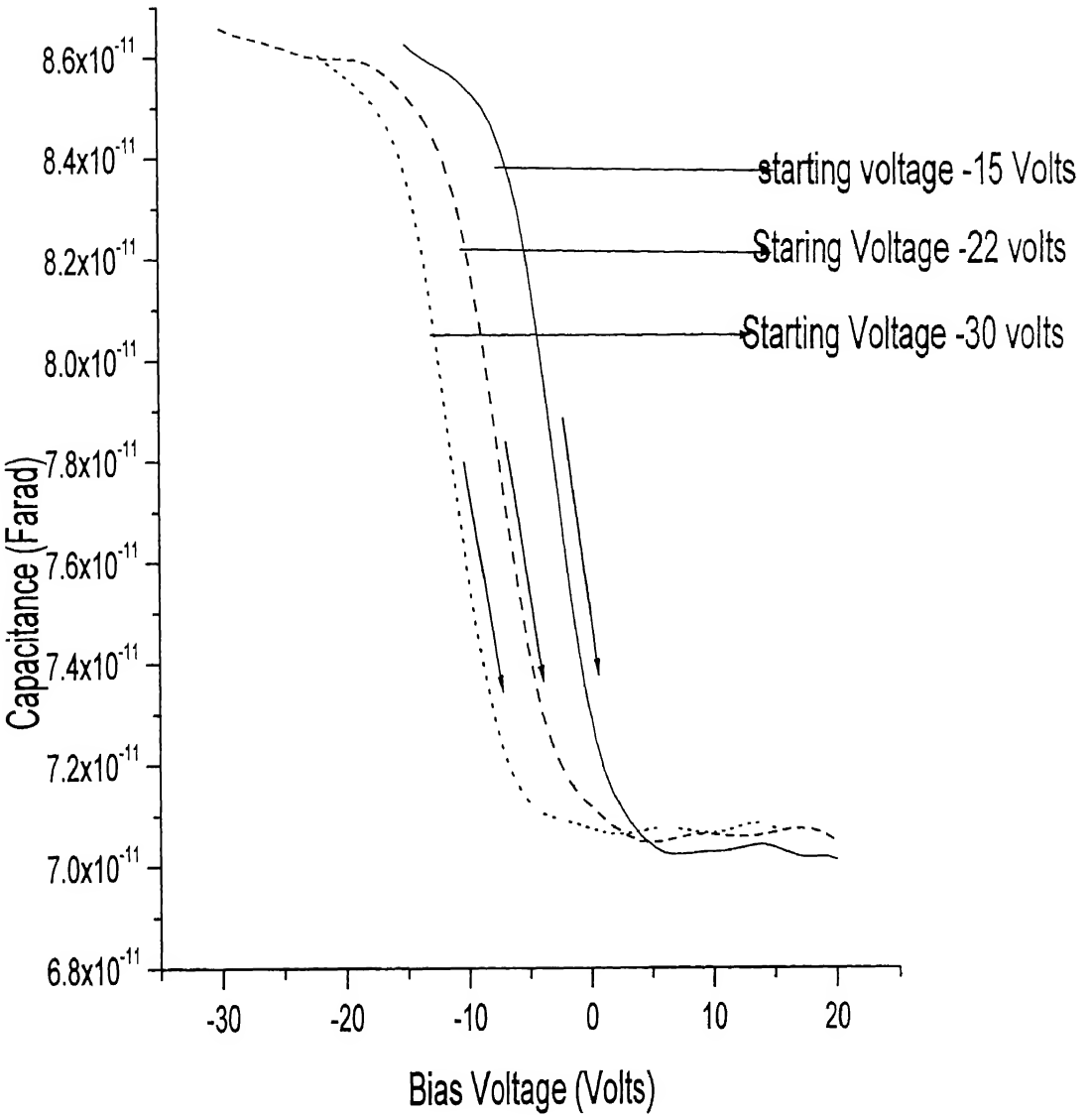


Figure 4.3 Effect of Starting Voltage on the Accumulation Region

4.3 Interface trap density

Interface trap density was measured using low-frequency (LF) C-V and conductance methods. Fig. 4.4 shows a typical HF and LF C -V curve for sample A1

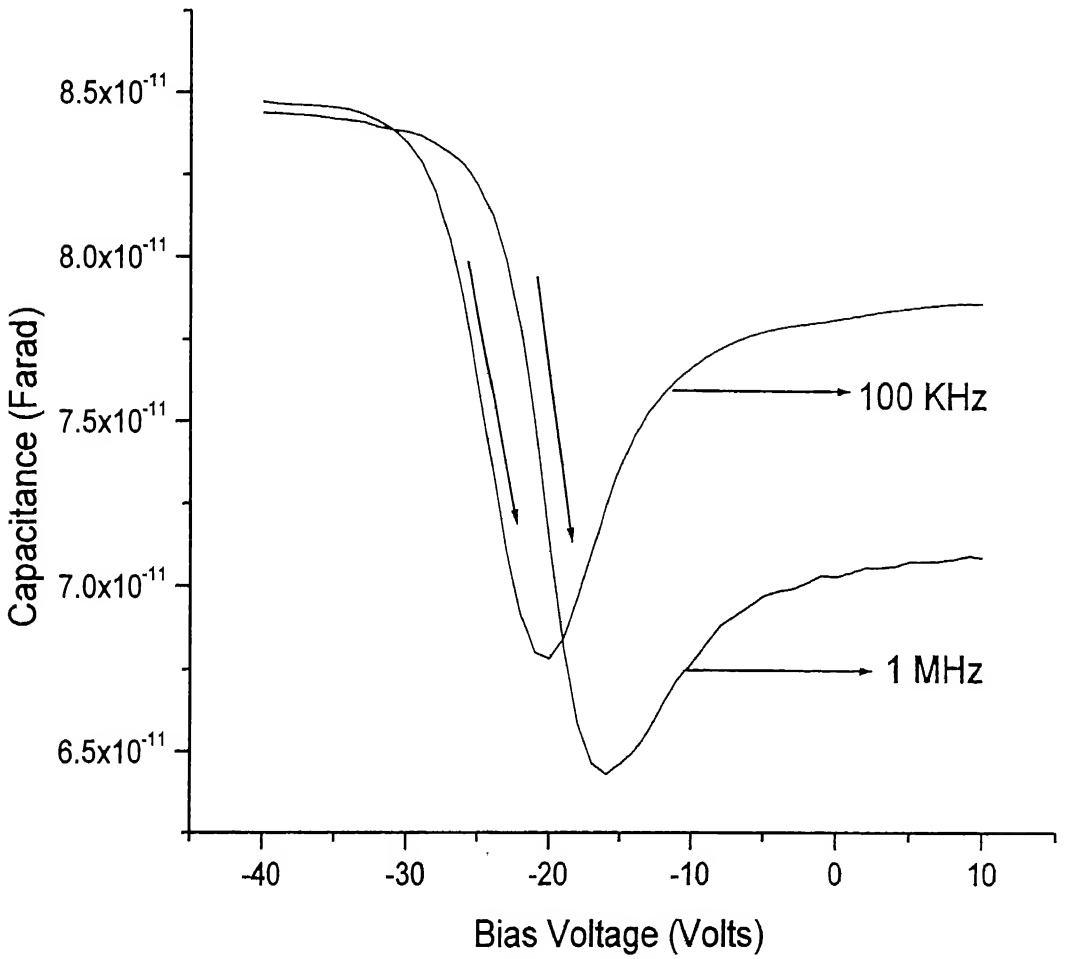


Figure 4.4 Effect of Frequency Change on C-V plot for sample A1

The conductance measurements were carried out with frequency as the sweep at 40 volts bias. Fig. 4.5 shows a typical conductance curve for sample A2. We have calculated D_{it} using the peak values from these curves, which will be the interface trap density close to the band edge, not the mid gap. Table 4.2 list the interface trap density calculated by the two methods. LF C -V method calculates the D_{it} value for

the mid -gap region, and conductance method calculates the D_{it} close to the band edge. To verify that the two methods are in agreement, D_{it} values were plotted as a function of the position in the band gap using LF C-V method in Fig 4.6. The D_{it} value for sample A1 near the band edge is 2.2 E12 by LF C-V method It is observed that D_{it} values for sample A4 is highest which is the thinnest sample grown in these experiments. There is no significant effect of the flow rate on the interface trap density.

Table 4.2 D_{it} values calculated using LF capacitance and conductance method.

Sample No	N_2O flow rate (ml/sec)	Time (Minutes)	D_{it} (C-V) ($Cm^{-2}eV^{-1}$)	D_{it} (G_p-F) ($Cm^{-2}eV^{-1}$)
A1	20	180	3.93E11	6.88E12
A2	25	150	4.59E11	1.82E12
A3	25	120	3.86e11	8.58E12
A4	20	45	2.81E12	1.15E13

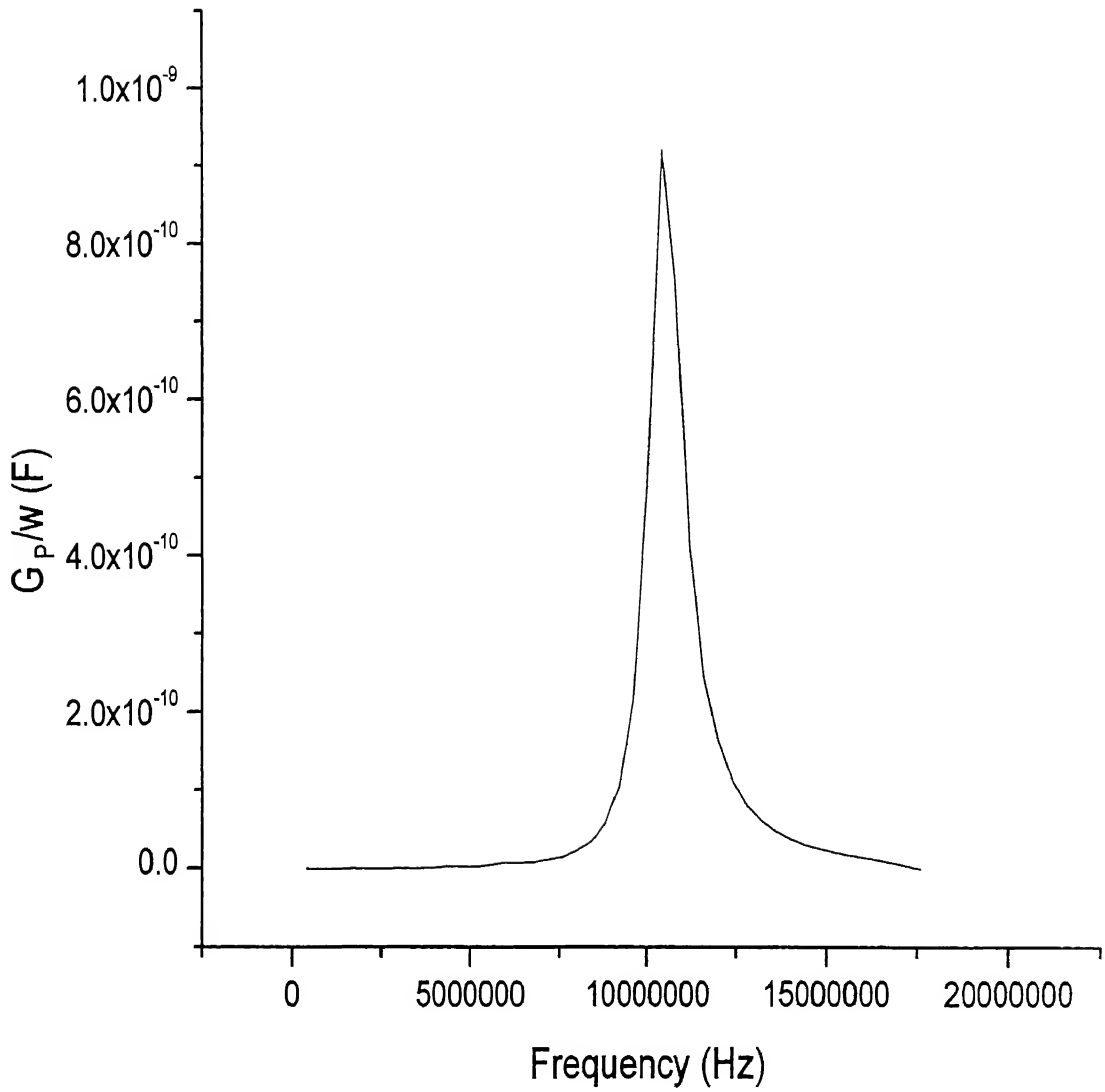


Figure 4.5 Conductance-frequency plot for sample A2 (Silicon Oxynitride oxidized for 150 minutes in N_2O at flow rate of 25ml/sec) at -40 Volts.

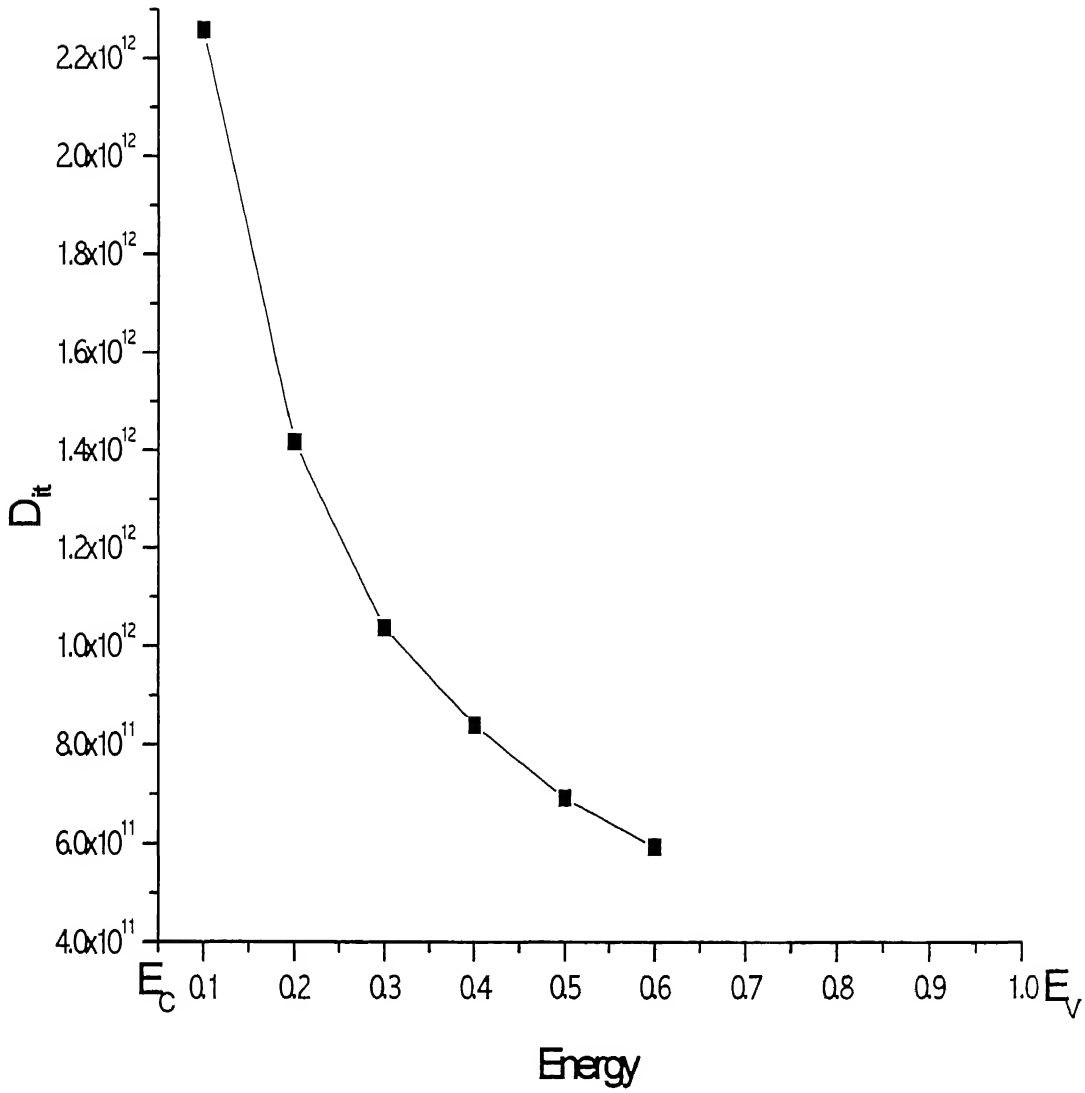


Figure 4.6 Interface trap level density as a function of bandgap energy

4.4I-V characteristics

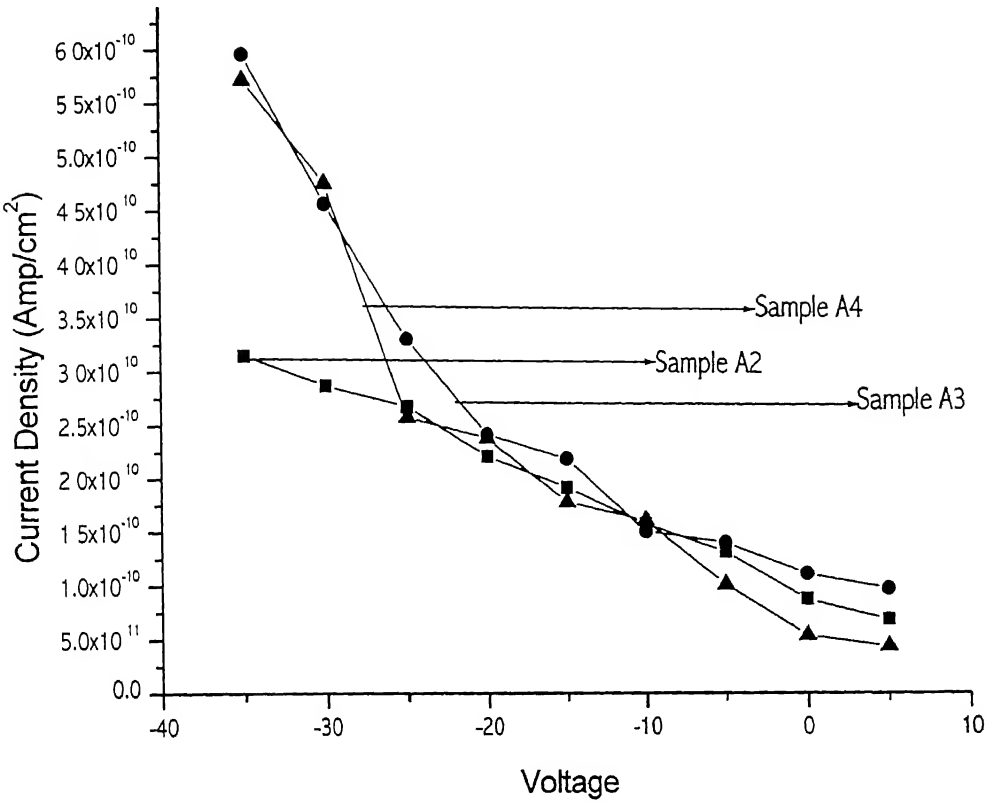


Figure 4.7 I-V plots for the samples A2, A3, and A4

The leakage current in our case is 10 orders of magnitude less compared to the leakage current in case of oxide grown under similar conditions. This difference is coming from the fact that the our films are 4-5 times thicker."

4.5 Film Composition

One of the unknown in SiO_xN_y is to find out how the N is incorporated in the film. Main difficulty is in finding a technique that can characterize the N content in the film and at the interface. FTIR spectroscopy has been successfully used to do this [41-42] We know from literature that Si-O antisymmetric stretch and bending modes are seen at 1070 cm^{-1} and 820 cm^{-1} respectively, and The Si-N peak is seen at about 854 cm^{-1}. It has been seen that with the incorporation of N the Si -O stretching mode peak shifts to lower wave numbers. Fig 4.8 and 4.9 shows the IR absorption spectra of samples A3 and A4 respectively. In the thicker SiO_xN_y film, the Si-O stretching mode is observed at 1081 cm^{-1} that is an indication of low dielectric constant around the Si-O bonds. Since normally the Si-strecth mode is seen at 1070 cm^{-1} in SiO_2, this indicates that effective dielectric constant around the Si-O bond is slightly less than 3.9 (dielectric const ant of the oxide). At the same time, it means that dielectric property of our films is similar to SiO_2, and there is very little N incorporation in the bulk film. This also supports our earlier conclusion that low dielectric constant measured by C-V is some sort of measurement effect. Lack of Si-N mode in the FTIR spectra supports this analysis.

Comparing the two films, it is observes that there is about 3 cm^{-1} shift of Si-O stretching mode (from 1081 to 1078) in the thinner film, which is an indicator for N incorporation at the interface compared to the bulk. Similar results have been reported by Chao. et al. [42]

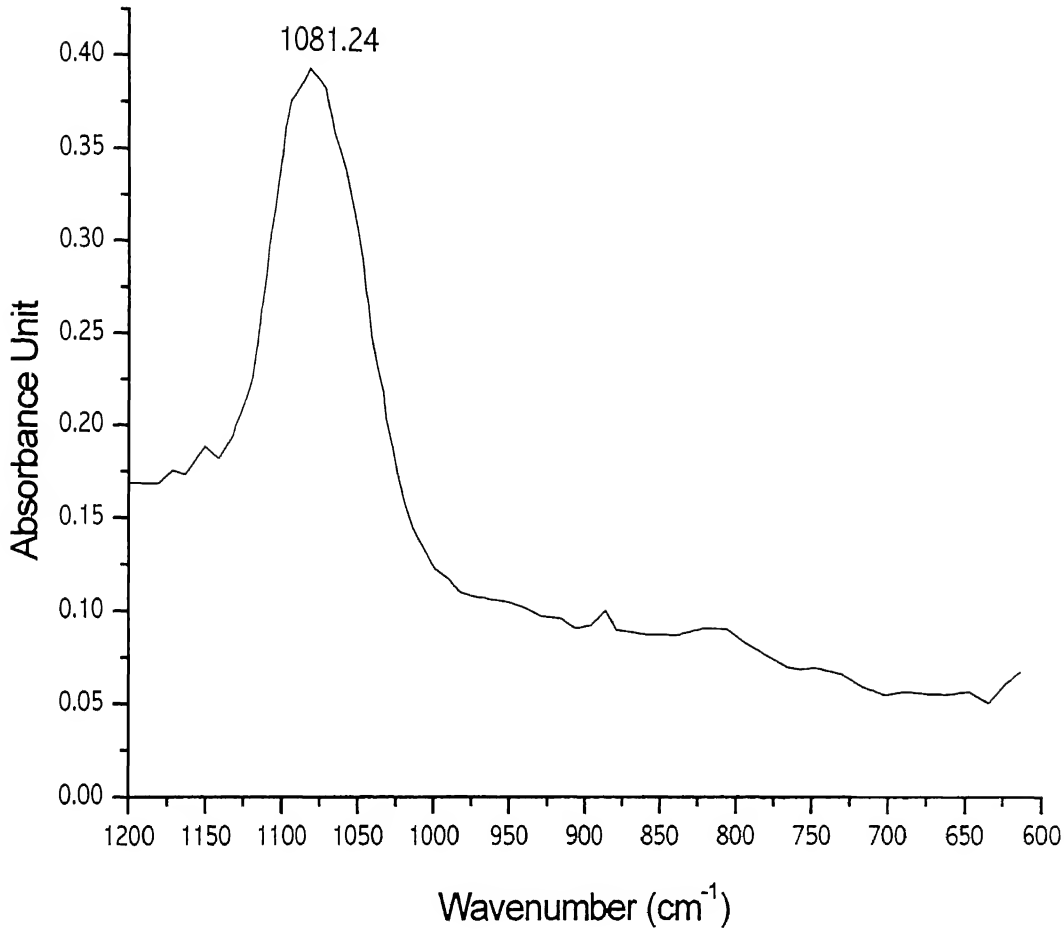


Figure 4.8 FTIR Spectra of sample grown in N_2O at 850°C for 2 Hrs and flow rate 25 ml/sec

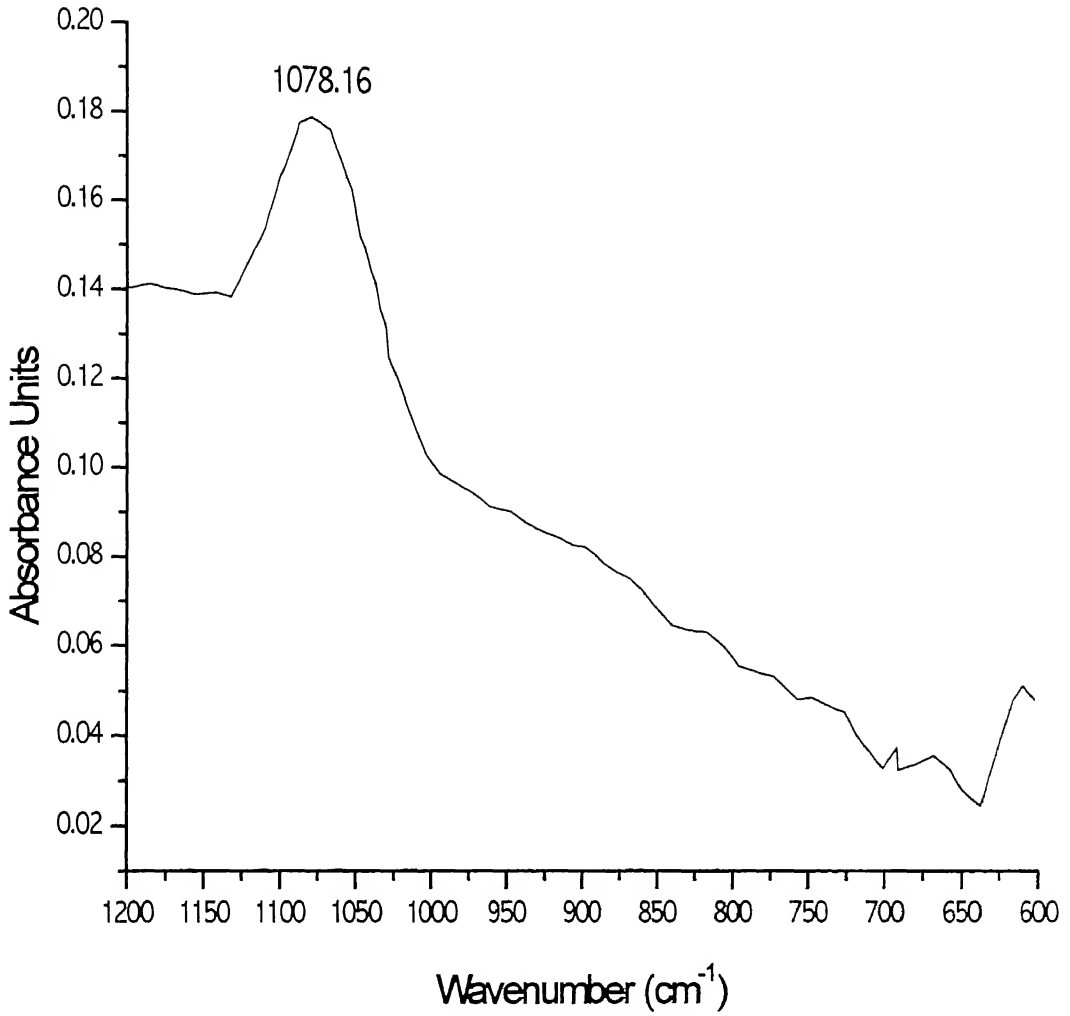


Figure 4.9 FTIR Spectra of simple grown in N_2O at 850°C for 45 min and flow rate 20 ml/sec

CHAPTER 5

Conclusions

In summary SiO_xN_y films were deposited by oxynitridation in N_2O atmosphere at 850^0C. Physical characterization of the films was done using ellipsometry and FTIR.MIS-C devices were fabricated and used for defect characterization in SiO_xN_y films. This preliminary study shows that further optimization of the processing conditions is required to improve the SiO_xN_y films before reliability studies can be undertaken. Main results of this work are presented below.

1. FTIR results show that we have very little incorporation of nitrogen in the SiO_xN_y as seen by absence of the Si-N modes. In addition to that Si-O stretching mode is seen at 1081 cm^{-1} in the bulk film, which should be around in 1040-1060 cm^{-1} range if there was substantial N incorporation in the film.
2. There is more N incorporation at the interface as compared to the bulk, as observed by the shift of Si-O mode to lower wave numbers in the thinnest film.
3. The interface trap density, D_{it}, in SiO_xN_y at mid-gap is about $\sim 10^{11}$ cm^{-2} eV^{-1}. This is quite good, considering interface trap density $< 5x10^{10}$ cm^{-2} eV^{-1} is needed for gate dielectrics.
4. The D_{it} measured by LF C-V method is in good agreement with the value obtained by the conductance method.
5. The D_{it} is low at the mid-gap and increases as we go towards the band edge.
6. There is considerable hystersis in the HF C-V curves that indicates large concentration of defects that act as electron traps.
7. Estimation of oxide defects density from the HF C-V curves also give 2-3 order of magnitude higher values compared to the value of device quality gate dielectrics.
8. The leakage current in our case is 10 orders of magnitude less compared to the leakage current in case of oxide grown under similar conditions. This difference is coming from the fact that the our films are 4-5 times thicker

9. There is some problem in the absolute value of the dielectric constant from CV plots, and it is probably coming from the device under test or measurement set-up. It is not a problem with SiO_xN_y as confirmed by the FTIR measurements.

REFERENCES

1. M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultrathin (<4nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits" J. Appl. Phys., vol. 90,No 5, pp. 2057-2121, 2001.
2. Shri Singhvi and Christos G. Takoudis, "Growth kinetics of furnace silicon oxynitridation in nitrous oxide ambients" J. Appl. Phys., vol. 82, No 1, pp. 442-448, 1997
3. H. C. Lu, E. P. Gusev, T. Gustafsson, and E. L. Garfunkel, "Effect of near interfacial nitrogen on the oxidation behavior of ultrathin silicon oxynitrides" J.Appl Phys., vol.81, No 10, pp.6992-6995, 1997.
4. DeWitt G. ONG, "Modern MOS Technology: Processes, Devices and Design", McGraw Hill, 1984.
5. E. P. Gusev, H. C. Lu, E. L. Garfunkel, T. Gustafsson, and M. L. Green, "Growth and characterization of ultrathin nitrided silicon oxide films" IBM J. Res.Dev, vol.43, No 3, pp.265-286, 1999.
6. A. Karamcheti, V. H. C. Watt, H. N. Al-shareef, T. Y. Luo, G. A. Brown, M. D.Jackson, and H. R. Huff, "Silicon Oxynitride Films as Segue to the high-K Era" Semiconductor FABTECH – 12th edition, pp 207-212.
7. G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations" J. Appl. Phys., vol.89, No.10, pp. 5243-5275, 2001.
8. Y. Ma, T. Yasuda, and G. Lucowsky, " Ultrathin device quality oxide-nitride-oxide heterostructure formed by remote plasma enhanced chemical vapor deposition"Appl. Phys. Lett, vol. 64, No 17,pp.2226, 1994
9. S. V. Hattangady, H. Niimi, and G. Lucovsky, "Integrated processing of silicon oxynitride films by combined plasma and rapid-thermal processing. Vac. Sci. Tecnol, vol. A14, No 6,pp. 3017-3023,1996
10. Y. Wu, and G. Lucovsky, " Ultrathin nitride/oxide (N/O) gate dielectrics for p^+-polysilicon gated PMOSFETs prepared by a combined remote plasma enhanced CVD/thermal oxidation process" IEEE Electron. Device Lett, vol.19, No.10, pp. 367-369, 1998.

11. R. Moazzami, and C. Hu, "A high-quality stacked thermal/LPCVD gate oxide technology for ULSI" IEEE Electron. Device Lett, vol. 14,No 2., pp.72-73, 1993.

12. P. K. McLarty, W. L. Hill, X. L. Xu, V. Misra, J. J. Wortman, and G. S. Harris, "Thin oxynitride film metal-oxide-semiconductor transistors prepared by low-pressure rapid thermal chemical vapor deposition" Appl. Phys. Lett, vol.63, No 26,pp 3619-3621, 1993.

13. D. Wang, T. P. Ma, J. W. Golz, B. L. Halpern, and J. J. Schmitt, "High-Quality MNS Capacitors Prepared by Jet Vapor deposition at Room Temperature"IEEE Electron Device Lett, vol.13, No13, pp.482-484, 1992.

14. H. Hwang, W. Ting, B. Maiti, D. L. Kwong, and J. Lee, "Electrical characteristics of ultrathin oxynitride gate dielectric prepared by rapid thermal oxidation of Si in N_2O Appl. Phys. Lett, vol 57,No10, pp.1010-1011, 1990.

15. H. Fukuda, T. Arakawa, and S. Ohno, "highly Reliable Thin Nitrided SiO_2 films Formed by Rapid Thermal Processing in an N_2O Ambient" Jpn. J. Appl. Phys., Part 2,vol 29,No.12 pp. L2333-L2336, 1990.

16. Y. Okada, P. J. Tobin, and S. A. Ajuria, IEEE Trans. Electron Devices, 41, 1608,1994.

17. K. Kumar, A. I. Chou, C. Lin, P. Choudhry, and J. C. Lee, "Optimization of sub 3 nm gate dielectrics grown by rapid thermal oxidation in a nitric oxide ambient"Appl. Phys. Lett, vol.70, No.3, pp. 384-386,1997.

18. Z. Q. Yao, "The nature and distribution of nitrogen in silicon oxynitride grown on silicon in a nitric oxide ambient. Appl. Phys., vol.78, No.5, pp. 2906-2912, 1995.

19. N. S. Saks, D. I. Ma, and W. B. Fowler, "Nitrogen depletion during oxidation in N_2O Appl. Phys. Lett, vol.67, No.3, pp. 374-376, 1995.

20. E. C. Car, K. A. Ellis, R. A. Buhrman, "N depth profiles in thin SiO_2 grown or processed in N_2O: The role of atomic oxygen" Appl.Phys.Lett, vol.66, No.12, pp. 1492-1494, 1995.

21. H. C. Lu, E. P. Gusev, E. L. Garfunkel, B. W. Busch, T. Gustafsson, T. W. Sorsch, and M. L. Green, "Isotopic labeling studies of interactions of nitric oxide and nitrous oxide with ultrathin oxynitride layers on silicon."J. Appl. Phys., vol. 87,No3 pp.1550-1555, 2000.

22. R. I. Hegde, P. J. Tobin, K. G. Reid, B. Maiti, and S. A. Ajuria, "Growth and surface chemistry of oxynitride gate dielectric using nitric oxide"Appl Phys. Lett, vol.66, pp.2882-2884, 1995.

23. M. Bhat, L. K. Han, D. Wristers, J. Yan, D. L. Kwong, and J. Fulford, "Effects of chemical composition on the electrical properties of NO-nitrided SiO_2" Appl. Phys.Lett, vol 66,No.10 pp.1225-1227, 1995.

24. H. C. Lu, E. P. Gusev, T. Gustafsson, E. L. Garfunkel, M. L. Green, D. Brasen, and L. C. Feldman. "High resolution ion scattering study of silicon oxynitridation"Appl. Phys. Lett, vol.69, No.18, pp. 2713-2715, 1996.

25. M. Bhat, D. Wristers, L. K. Han, J. Yan, H. J. Fulford, and D. L. Kwong, "Electrical Properties and Reliability of MOSFET's with Rapid Thermal NO-Nitrided SiO_2 Gate Dielectrics" IEEE Trans. Electron Devices, vol.42, No5, pp 907-914, 1995.

26. K. A. Ellis, R. A. Buhrman, "Furnace gas-phase chemistry of silicon oxynitridation in N_2O" Appl. Phys. Lett, vol 68,No12, pp. 1696-1701, 1996.

27. M. L. Green, D. Brasen, K. W. Evans-Lutterodt, L. C. Feldman, K. Krisch, W.Lennard, H. T. Tang, L. Manchanda, and M. T. Tang, "Rapid thermal oxidation of silicon in N_2O between 800-1200^{0}C: Incorporated nitrogen and interfacial roughness" Appl. Phys. Lett, vol 65,No.7, pp. 848-850, 1994.

28. M. Y. Hao, D. Nayak, and R. Rakkhit, "Impact of boron penetration at P^+-poly/gate oxide interface on deep-submicron device reliability for dual-gate CMOS technologies" IEEE Electron Device Lett, vol.18, No.5, pp. 215217, 1997.

29. D. Mathiot, A. Straboni, E. Andre, and P. Debenest, "Boron diffusion through thin gate oxides: Influence of nitridation and effect on the Si/SiO_2 interface electrical characteristics. Appl. Phys., vol73, No 12, pp.8215-8220, 1993.

30. J.Vuillod, "Preparation and characterization of plasma enhanced chemical vapor deposited silicon nitride oxynitride films. Vac.Sci.tecnol. vol. A 5,No. 4,pp.1675-1677, 1987.

31. L.Torrison, J.Tolle, J.Kouvetakis, S.K.Dey, D.Gu, I.S.T.Tsong, P.A.Crozier. "Stoichiometric and non-stoichiometric films in the Si-O-N system: mechanical, electrical, and dielectric properties" Material Science and Engineering, vol B 97,pp.54-58, 2003

32. E. H. Nicollian and J. R. Brews, MOS Physics and Technology, Wiley, New York, 1982.

33. Dieter K. Schroder, "Semiconductor Material and Device Characterization", Weily, New York, 1990.

34. M. Bhat, H. H. Jia, and D. L. Kwong, "Growth kinetics of oxides during furnace oxidation of Si in N_2O ambient" J. Appl. Phys., vol. 78, No 4, pp.2767-2774, 1995.

35. W.Ting, H.Hwang, J.Lee, and D.L.Kwong, "Composition and growth kinetics of ultrathin SiO_2 formed by oxidizing Si substrates in N_2O"Appl.Phys.Lett, vol 57, No.26, pp2808-2810, 1990

36. M. Bhat, L. K. Han, D. Wristers, J. Yan, and D. J. Kwong, "Effects of chemical composition on the electrical properties of NO–nitrided SiO_2"Appl. Phys. Letter, vol.66, No10, pp1225-1227, 1995

37. Z. Wu, Z. Shiung, C. Chiang, W. Wu, M. Chen, S. Jeng, W. Chang, P. Chou, S. Jang, C. Yu, M. Liang, "Physical and electrical characteristics of G- and C - Doped low dielectric constant chemical vapor deposited oxides", J. Electrochem. Soc., 148(6) F115-F119, 2001.

38. Z. Wu, Z. Shiung, C. Chiang, W. Wu, M. Chen, S. Jeng, W. Chang, P. Chou, S. Jang, C. Yu, M. Liang, "Physical and electrical characteristics of methylsilane – and trimethylsilane- doped low dielectric constant chemical vapor deposited oxides", J.Electrochem. Soc., 148(6) F127-F132, 2001.

39. J, Zhang, I. Boyd, "Low dielectric constant porous silica films formed by photo-induced sol-gel processing", Mat. Sci. Sem. Proc. 3, 345-349, 2000

40. W. Cho, R. Kosugi, J. Senzaki, K. Fukuda, K. Aai, S. Suzuki, "Study on electron trapping and interface states of various gate dielectric materials in 4H-SiC metal-oxide-semiconductor capacitors"

41. E.Desbiens, R. Dolbec, M.A El Khakani, "Reactive pulsed laser deposition of high-k silicon dioxide and silicon oxynitride thin films for gate-dielectric applications", J. Vac. Sci. Technol., vol A 20,No.3, pp. 1157-1161, 2002.

42. S.M.Sze, "Physics of Semiconductor Devices" Wiley, New York, 1981

43. T.S. Chao, W.H. Chen, T.F. Lei, "Fourier Transform Infrared Spectroscopic Study of Oxide Films Grown in Pure N_2O", Jpn. J. Appl Phys., vol.34, pp. 2370-2373, 1995

Appendix A

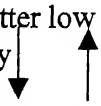
1. C-V Measurement Operation Procedure:

The Agilent 4294A Precision impedance Analyzer is can be used for electrical characterization. W can measure absolute impedance, resistance, capacitance, conductance, and inductance of a circuit by selecting appropriate category. Following is the procedure to operate the impedance analyzer:

1. Turn on the power. Wait for some time to see the display "Power on self Test in progress".
2. After this test is successful, measurement screen appears on the LCD.
3. For the Agilent to perform the measurement, we must select the appropriate adapter type option. Whenever we start a new measurement session, we should check the indicator for ("EX1," "EX2", "7mm," or blank) shown in the instrument status area to confirm that the correct type is selected.
4. Press the **[Preset]** key to initialize the Agilent 4294A.
5. To select the measurement parameters press the **[Meas]** key to display Measurement parameter menu.
6. Select the desired parameter e.g. for impedance and phase measurement measurement select the Z-□ parameter. Trace A gives the absolute impedance while Trace B reflects the impedance phase.
7. For selecting the sweep press the **[Sweep]** key to display sweep menu.
8. Check the **PARAMETER** [] soft key to confirm that desired sweep is selected by seeing the desired sweep shown between the brackets **[].**
9. From the Sweep menu, select the **TYPE** [] to display the Sweep type menu. Select the **LIN** or **LOG** to select the Linear or Log Sweep.
10. Set the Sweep start value to desired value by pressing the [**START**] key and enter the desired value. Similarly for Sweep stop set the desired value.
11. Perform the open calibration before taking any measurement. For open measurement press the **[CAL]** key and then press the open key.
12. Connect the device and take the measurement.

2. **I-V Measurement Operation Procedure:**

The Keithley's 6172 model can be used for various tests like resitivity, leakage current and estimating voltage (current) by supplying current (voltage). For measuring the current we need to do perform the following configuration

1. Power on the machine.
2. Zero check displays on the LCD.
3. For internal emitter low connection press the "config" then press arrow up and down key 
4. Go to meter connect option. Using
5. Select meter connect by pressing enter.
6. Go to on state and press enter, and then press exit.
7. Now apply the desired voltage and then press operate to see the current.

Appendix B

B1 C-V Curves

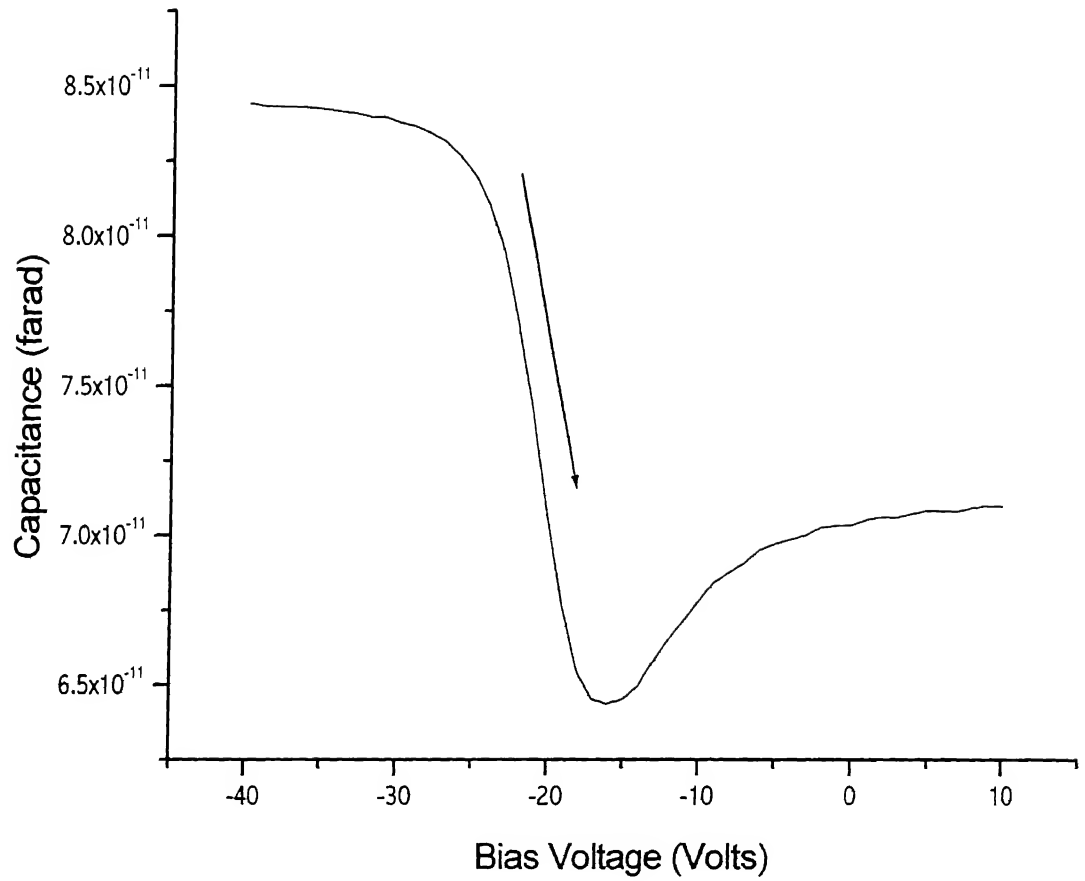


Figure B.1 C-V plot for sample A1 (Silicon Oxynitride oxidized for 180 minutes in N2O at flow rate of 20ml/sec) at 1 MHz.

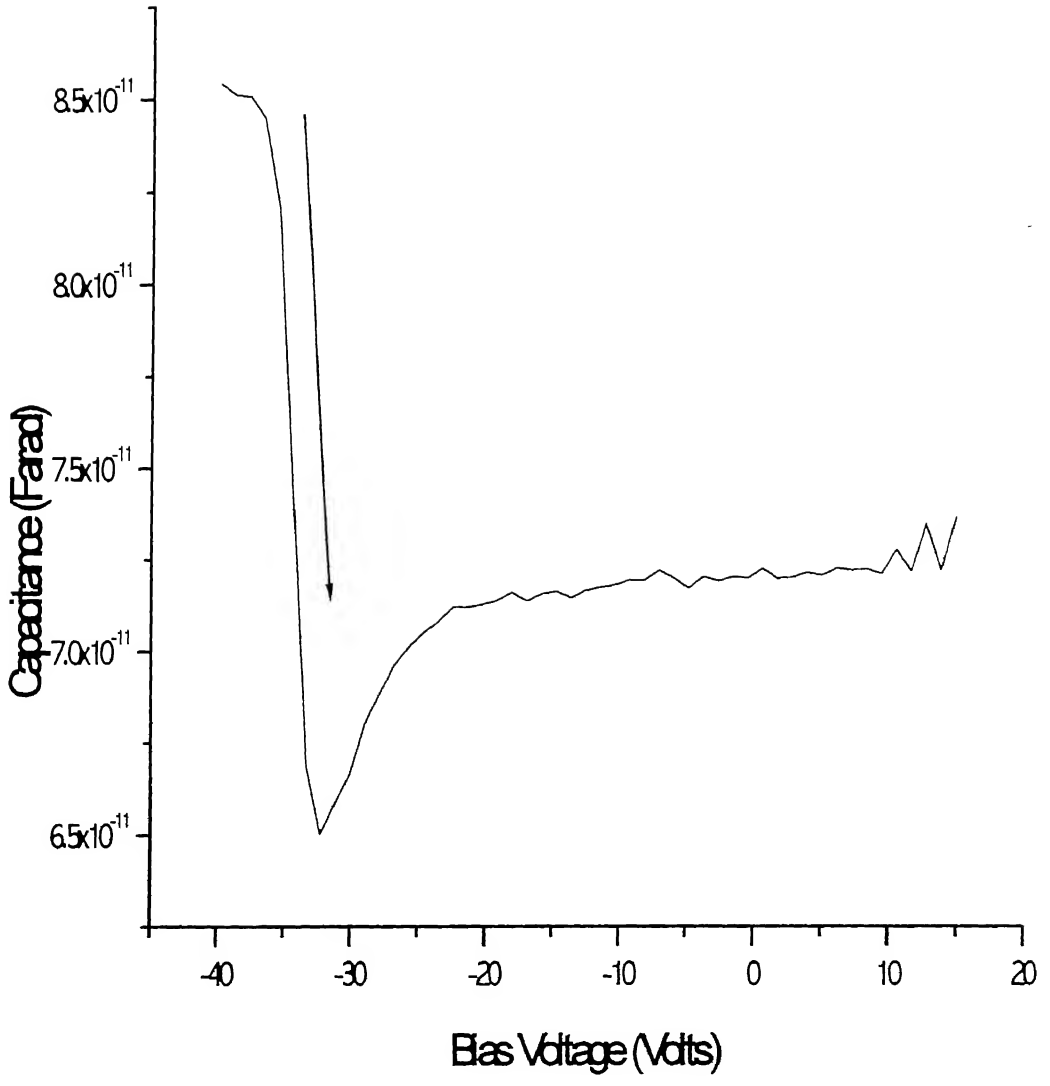


Figure B.2 C-V plot for sample A3 (Silicon Oxynitride oxidized for 120 minutes in N2O at flow rate of 25ml/sec) at 1 MHz.

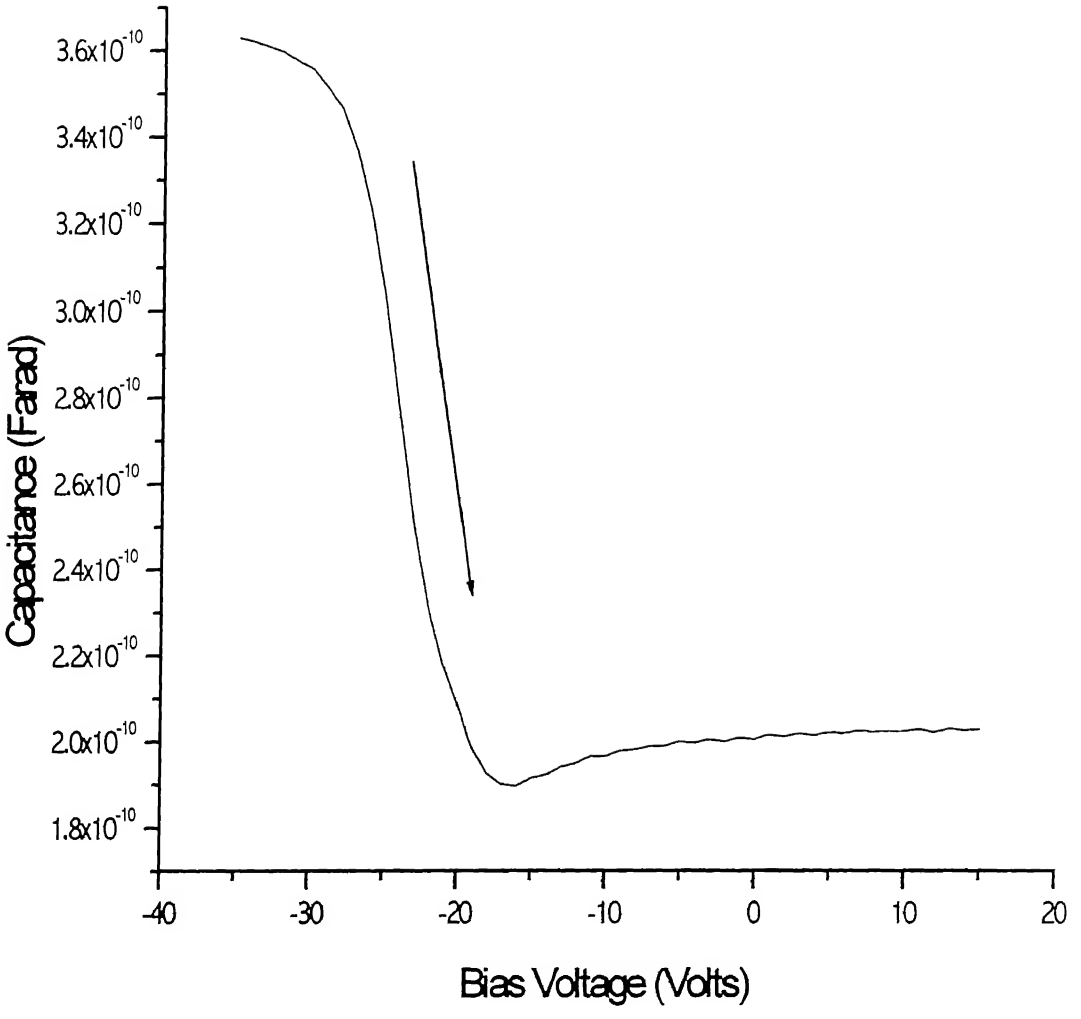


Figure B.3 C-V plot for sample A4 (Silicon Oxynitride oxidized for 45 minutes in N2O at flow rate of 20ml/sec) at 1 MHz.

B2 Conductance Curve

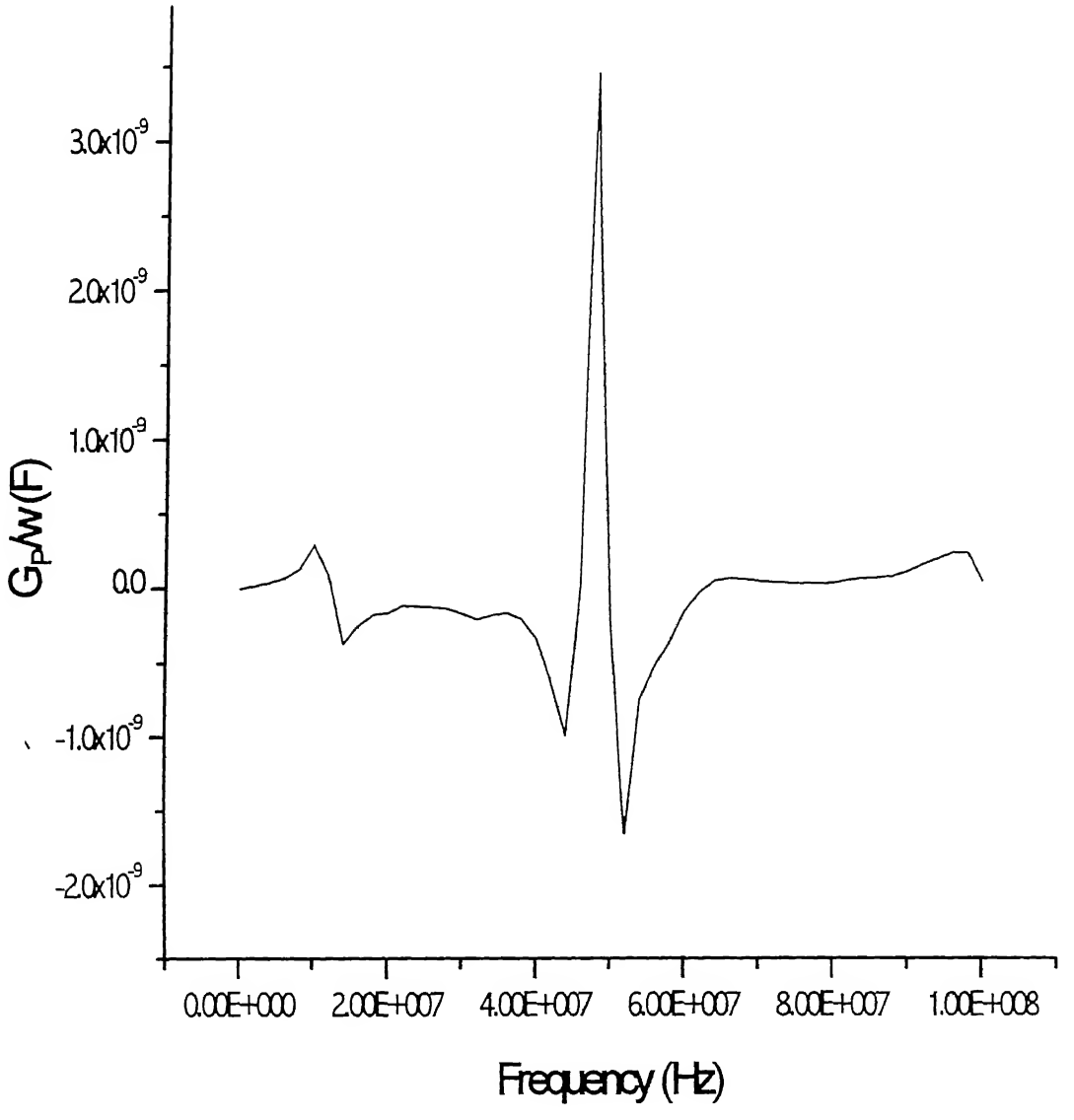


Figure B.4 Conductance-frequency plot for sample A1 (Silicon Oxynitride oxidized for 180 minutes in N_2O at flow rate of 20ml/sec) at -40 Volts

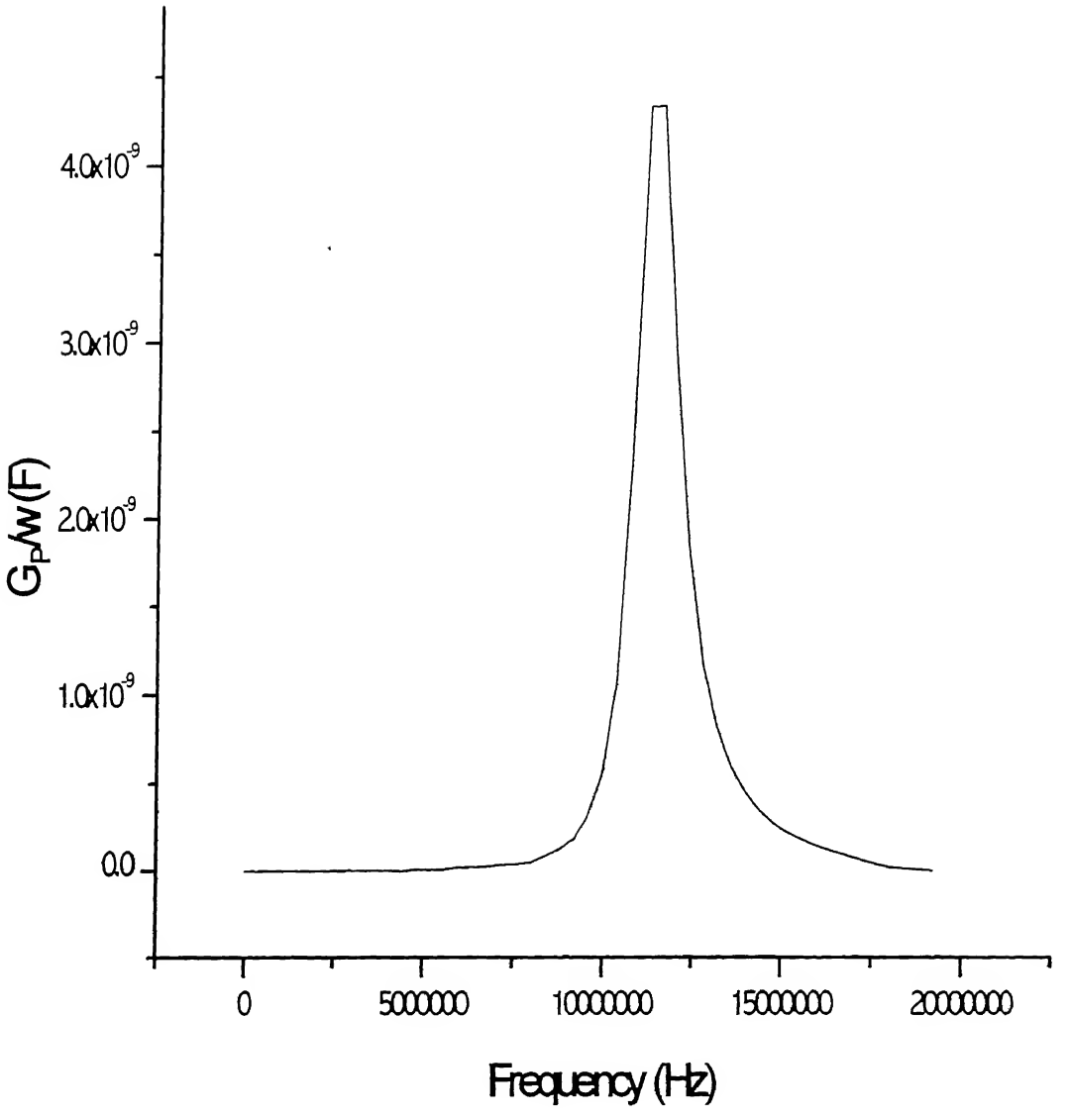


Figure B.5 Conductance-frequency plot for sample A3 (Silicon Oxynitride oxidized for 120 minutes in N_2O at flow rate of 25ml/sec) at -40 Volts

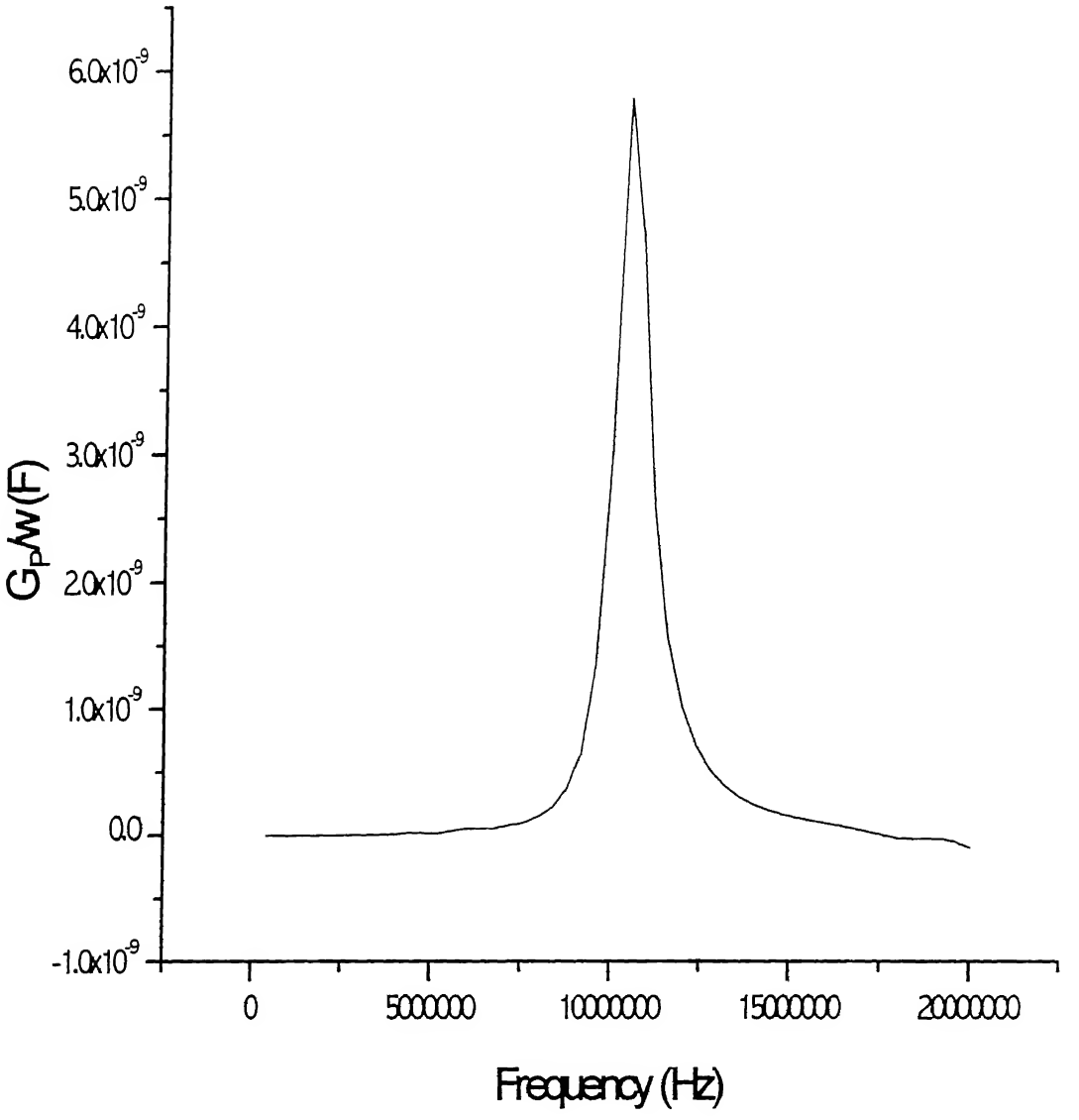


Figure B.6 Conductance-frequency plot for sample A4 (Silicon Oxynitride oxidized for 45 minutes in N_2O at flow rate of 20ml/sec) at -40 Volts